Built - In Self Test insertion in a System On a Chip

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• BIST IN GENERAL
• DESIGN DESCRIPTION
• RAM BIST DESIGN FLOW
• RAM BIST VERIFICATION
• PIN REQUIREMENTS
• RAM BIST OPERATION
• PROBLEMS ENCOUNTERED
• TEST STATISTICS - CONCLUSIONS
• added test circuitry carries out the test and gives the final pass/fail result,
• to achieve the best fault coverage circuitry specific test vectors are in use
DESIGN DESCRIPTION - SYSTEM ON A CHIP FOR TELECOMMUNICATIONS PURPOSES

200k gates DECT basestation
ARM subsystem
DFT: scan test, IDDQ, boundary scan, ARM test, nand tree test, BIST

RAMs on board:

- 1 x 5120 words, 8 bit RAM
- 5 x 2048 words, 8 bit RAMs
- 4 x 64 words, 8 bit RAMs
- 1 x 64 words, 8 bit 2 port RAM
- 1 x 64 words, 9 bit 2 port RAM
BIST’ed MEMORY REPLACES RAM

BIST - Built In Self Test
<table>
<thead>
<tr>
<th>ADVANTAGES</th>
<th>DISADVANTAGES</th>
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<tbody>
<tr>
<td>• high fault coverage</td>
<td>• silicon area overhead</td>
</tr>
<tr>
<td>• test mode can be switched on whenever it is necessary</td>
<td>• extra pins or multiple pins required</td>
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<td>• shorter test times - memories can be tested in parallel</td>
<td>• memory access time - extra steering logic</td>
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<td>• reusability, repeatability</td>
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<td>• embedded RAMs with no direct access to pins can be tested</td>
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<tr>
<td>• lower cost of the test</td>
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BIST RELATED SUPPLIES from MEMORY CORE PROVIDER

RAM VHDL
models
synthesis scripts

BIST package - RTL
RAMtype_bist_collar.vhd
bist_cntrl.vhd
bist_assembly.vhd
bist_testbench.vhd

Simulation files
bist_testbench.vhd
_collar_config_syn.vhd
bist_config.vhd
BIST INSERTION - DESIGN FLOW

- automatic RAM generation tool
  - VHDL/Verilog sim. model
  - generated RAM model
  - generated config file

- BIST generator
  - VHDL/Verilog sim. stimulus
  - Synopsys script
  - RAM BIST RTL

- SYNOPSIS
  - RAMBIST netlist

- TO DESIGN
  - VHDL/Verilog simulator
  - BIST VERIFICATION

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BIST VERIFICATION

The goal of verification is to check if the Synopsys synthesized RAM BIST circuitry operates with the RAM properly. This was done with generated RAM simulation model.

During verification BIST - generated testbenches were used to simulate RAM BIST circuitry.

The testbench enables BIST mode and monitors status signals.
BIST HIERARCHY

<RAM_name>bist_cntrl

BIST Controller

<RAM_name>BIST-collar

RAM

BIST Collar

<RAM_name>BIST_assembly

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**BIST PINS AND SIGNALS**

- **BIST_CLK**: common clock for the RAM and all BIST modules.
- **BIST_EN**: turns the BIST mode on, a controller activation.
- **TMS**: collar’s transparent mode activation.
- **BIST_DONE**: test completed.
- **BIST_CMP_STAT**: bit by bit compare status.
- **BIST_GO**: test passed/failed, latched to 0 if the first error has been detected.
- **BIST_ON**:
RAM WITH BIST CIRCUITRY

BIST CONTROLLER

BIST EN
BIST_RST
BIST_CLK
TMS
TEST_SI
TEST_SE

BIST_ON
BIST_COMP_STAT
BIST_DONE
BIST_GO

TEST_SO

64x8 RAM

adrress
bus

ADR [5:0]

R
W
WEN

Data IN [7:0]

DIN [7:0]

CLK

Data OUT [7:0]

Dout [7:0]

BIST COLLAR

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TOP LEVEL BIST CONNECTIONS

PADS

TEST BL

BIST_DONE
BIST_CMP_STAT
BIST_CLK
BIST_EN

BIST_CLK
BIST_EN
TMS

block A
BIST cntrl

64B RAM
BIST

block B BIST
cntrl

4x64B RAM
BIST

block C BIST
cntrl

4x2kB, 1x5kB RAM
BIST

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PIN REQUIREMENTS

4 BIST SIGNALS ARE REQUIRED TO BE ACCESSIBLE DIRECTLY FROM PINS

• BIST_CLK,
• BIST_EN,
• BIST_DONE,
• BIST_CMP_STAT

PINS WHICH CAN NEVER BE USED FOR BIST SIGNALS

• ASYNCHRONOUS RESET,
• DEDICATED TAP CONTROLLER PINS
• BIDIRECTIONAL AND OUTPUT PINS WITH CRITICAL TIMING NOT ACCEPTING ADDITIONAL MUX DELAY
The deterministic SMARCH algorithm was implemented.

The algorithm consisted of the following steps:

\[ (R_{0/1-0}W_{1-0}); (R_{1-0}W_{0-0}); \uparrow(W_0); \uparrow(R_0W_1) \uparrow(R_1W_0); \]
\[ \downarrow(R_0W_1); \downarrow(R_1W_0); \downarrow R_0 \]

The following types of faults are being detected:

• Stuck-at faults (SAF),
• Coupling faults - shorts between cells, static coupling,
• Multi Access faults - shorts between address/data lines,
• Transition faults,
• Data Retention faults.
PROBLEMS ENCOUNTERED

• collar functionality - no multiplexers for BIST_CLK going to RAM during the test,
• all the data to the RAM’s in BIST mode was set up by the BIST controller on the rising edge of BIST_CLK
• bugs in automatically generated wrappers
### MEMORY TEST TIME

<table>
<thead>
<tr>
<th>Block of RAM</th>
<th>1 x 64B</th>
<th>1 x 2kB</th>
<th>4x2kB, 1x5kB</th>
</tr>
</thead>
<tbody>
<tr>
<td>TEST TIME</td>
<td>5930</td>
<td>188458</td>
<td>1224898</td>
</tr>
<tr>
<td>clock cycles</td>
<td></td>
<td></td>
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</tbody>
</table>

### BIST AREA OVERHEAD

![BIST area overhead chart]

- BIST area overhead
  - Blocks of RAMs:
    - 1x2kB
    - 4x2kB + 1x5kB
    - 4x64
    - 1x64B
    - Total
CONCLUSION

• BIST - an efficient tool to test RAMs,
• reduces test time and costs,
• tests can be done during the operational life of a chip,
• suitable for SoC - in designs where there is no direct access to pins,
• BIST was implemented by replacing RAMs with BIST’ed memories,
• BIST area overhead was 10.5% which is acceptable,
• delay caused by additional MUXes is not significant
THANK YOU