Sunday May 21, 2006

09:00-17:00	**Full-Day Tutorials** *Organizer: Peter Harrod (ARM, UK) – ETS'06 Tutorial Chair* *Organized in cooperation with TTTC's Test Technology Educational Program (TTEP)*	Univ. of Southampton

Tutorial 1:
DFM, DFT, Silicon Debug and Diagnosis – The Loop to Ensure Product Yield
Presenters: Srikanth Venkataraman (Intel, US)
Nagesh Tamarapalli (Mentor Graphics, US)

Targeted Audience: Designers; test, DfT and product engineers; validation, yield, debug and failure analysis engineers; researchers; students and managers, and anyone who is interested in learning about state-of-the-art DfM, manufacturing test, debug and diagnosis methodologies that are being employed today across the industry.

Abstract: Semiconductor yield has traditionally been limited by random particle-defect based issues. However, as the feature sizes reduced to 0.18 μm and below, systematic mechanism-limited yield loss began to appear as a substantial component in yield loss due to the interaction between design and manufacturing. This tutorial covers the following topics. Design-for-Manufacturing (DFM) techniques to analyze the design content, flag areas of design that could limit yield, and make changes to improve yield. Test techniques to close the loop by crafting test patterns to expose the defect prone features during automatic test pattern generation (ATPG) and by analyzing silicon failures through diagnosis to determine the features that are actually causing yield loss and their relative impact. Design techniques (DFX) to improve testability, debuggability and diagnosability. Both basic concepts and theoretical aspects of debug and diagnosis are covered. The application of statistical diagnosis techniques to determine the features that are actually causing yield loss and their relative impact is presented.

Keywords: Design-for-Manufacturing, yield, feature-limited yield, DfM rule deck, reticle enhancement technology (RET), optical proximity correction (OPC), phase-shift masking (PSM), lithography, Design-for-Test (DfT), defects, defect-level, fault models, scan, ATPG, BIST, memory BIST, at-speed tests, DfM-oriented test, compressed test, silicon debug, diagnosis, scan chain diagnosis, logic diagnosis, at-speed diagnosis, high-volume statistical diagnosis, yield management systems.

Tutorial 2:
Delay-Fault Testing: From Basics to ASICs
Presenters: Ben Bennetts (Bennetts Associates, UK)
Bram Kruseman (Philips Research, NL)

Target Audience: Designers, test engineers and researchers interested in understanding and using delay-fault testing for the detection of defects.

Summary: At-speed testing of digital ICs using internal scan chains and targeted on propagation-delay faults is becoming a mainstream test method whose usage is no longer limited to high-speed ICs. Nowadays, it is a requirement for any IC manufactured in an advanced technology to obtain acceptable at-speed functional behaviour and manufacturing quality levels. This tutorial covers all aspects of at-speed testing for delay faults: starting with the basic causes of delay-fault failure mechanisms, and continuing with pattern generation and application protocols for at-speed test through scan chains, associated design-for-testability requirements, and implementation in a test program including meaningful analysis of the test responses. We will share industrial experiences as well as research directions to refine at-speed testing even further.

Keywords: Delay-fault test, hard and weak shorts and opens, fault models, ATPG, design-for-test, shmoo plots, delay mapping, clocking issues.

Monday May 22, 2006

08:30-10:00	**Session 1: Plenary Opening** *Moderator: H.-J. Wunderlich (Univ. Stuttgart, DE) – ETS'06 Vice Program Chair*	Library Suite
08:30	Welcome Address *B.M. Al-Hashimi (Univ. of Southampton, UK) – ETS'06 General Chair*	
08:40	Keynote: Innovation and Wealth Creation from Technology *R. Saxby (ARM, UK)*  Innovation is a key driver in today's high technology businesses. But what is innovation? And what does it take to turn a good idea into a business success story? In this talk I'll take a look at a number of innovative products and show what's made them into winners. And by using ARM as an example, I'll describe how a business can be built around innovation and how ARM developed a unique business model to exploit its key advantages. But once a company is successful, how do you maintain a competitive advantage? I'll describe how a culture for innovation can be developed – and then look at where innovation might take us with a glimpse into the future. This will include a brief look at the critical importance of innovations in the field of test to the success of the processor core business as we move into the era of 65nm and below. *Speaker Biography* Sir Robin Saxby was involved in founding ARM and joined the company full-time in February 1991 as President and Chief Executive Officer, becoming Chairman in October 2001. Prior to ARM, he was with ES2, Motorola Semiconductors, and Henderson Security Systems Limited. He has also served as Chairman of the Open Microprocessor Initiative Advisory Group, which advised on collaborative R&D activity within Europe. He holds a BEng in Electronics and is a chartered engineer, Hon FIEE and FREng. He has received an honorary doctorate from the University of Liverpool where he is a Visiting Professor, has honorary doctorates from Loughborough University and the University of Essex, and has received the Faraday Medal of the IEE (Institution of Electrical Engineers). He was knighted in the 2002 New Year's Honours List. He currently serves as Deputy President of the IEE, where he is also a trustee. He is a non-executive director of Glotel plc.	
09:10	Presentation of ETS'05 Best Paper Award *M. Renovell (LIRMM, FR) – ETS'05 Program Chair*	
09:15	Invited Address: Living with Failure: Lessons From Nature? *S. Furber (Univ. of Manchester, UK)*  Industry predictions suggest that within a decade we will see 100 billion transistor chips. The bad news is that 20 billion of those transistors will fail in manufacture and a further 10 billion will fail in the first year of operation. What does a 20-30% device failure rate mean for designers and for production test? Standard fault-tolerant design assumes that faults are infrequent; a 20-30% failure rate violates this assumption. For an example of a functional device that can cope with this level of failure we must look to nature. Brains cope with high levels of neuron failure. But we have no idea how they work, let alone how they keep working after these failures. What might we learn from biology about building systems that continue to function as components change and fail? How can we design future production tests to establish that enough of a chip works for it to be useful, and will continue to be useful after further early-life failures? *Speaker Biography* Steve Furber is the ICL Professor of Computer Engineering in the School of Computer Science at the University of Manchester. He received his B.A. degree in Mathematics in 1974 and his Ph.D. in Aerodynamics in 1980 from the University of Cambridge, England. From 1980 to 1990 he worked in the hardware development group within the R&D department at Acorn Computers Ltd, and was a principal designer of the BBC Microcomputer and the ARM 32-bit RISC microprocessor, both of which earned Acorn Computers a Queen's Award for Technology. He took up the ICL Chair at Manchester in 1990 where he now leads the EPSRC-funded Advanced Processor Technologies Portfolio Partnership. Steve is a Fellow of the Royal Society, the Royal Academy of Engineering, the British Computer Society, the Institution of Electrical Engineers and the IEEE. In 2003 he was awarded a Royal Academy of Engineering Silver Medal, and in 2004 became the holder of a Royal Society-Wolfson Research Merit Award.	

09:45	Introduction to ETS'06 Technical Program *E.J. Marinissen (Philips Research, NL) – ETS'06 Program Chair*
09:55	Practical Aspects of ETS'06 *M. Zwolinski (Univ. of Southampton, UK) – ETS'06 Local Arrangements Chair*

10:00-11:00	**Session 2: Posters and Coffee/Tea Break**	**Avon**	
	Input Cones Based on Test Sequences for Synchronous Sequential Circuits *I. Pomeranz (Purdue Univ., US), S. Reddy (Univ. of Iowa, US)*		
	Strengthening Logic BIST with IDDQ - Taking the Best of Both Worlds *J.S. Vaccaro, T. Colunga, L. Benecke, S. Mahadevan (Freescale Semiconductor, US), H. Manhaeve (Q-Star Test, BE)*		
	Extended Compatibilities for Scan Tree Construction *Z. You, M. Inoue, H. Fujiwara (Nara Inst. of Science and Tech., JP)*		
	Proposal of a Clock Signal Generation/Detection Method for Crosstalk Aware Design *Y. Miura (Tokyo Metropolitan Univ., JP)*		
	Efficient and Accurate Analog Sinewave Generator for BIST Applications *M.J. Barragán, D. Vázquez, G. Huertas, A. Rueda, J.L. Huertas (Univ. de Sevilla, ES)*		
	Some Improvements of Phase-Spectrum ADC Hysteresis Test for Practical Application *D. Slepička, D. Dallet (Laboratoire IXL, FR), V. Shitikov, F. Barbara (Schlumberger, FR)*		
	Bitline-Coupled Precharge Faults and Their Detection in Memory Devices *Z. Al-Ars, S. Hamdioui (Delft Univ. of Tech., NL), G. Müller, J. Vollrath (Infineon Technologies, DE)*		
	Automatic Test Program Generation Tool for Mixed-Signal Device Interface Boards *B.C. Kim (Univ. of Alabama, US), V. Kalyanaraman, P. Variyam (Texas Instruments, US), S. Cherubal (WiQuest Communications, US)*		

11:00-12:30	**Session 3A: Delay Fault Testing** *Moderators: W. Anheier (Bremen Univ., DE)* *A. Majhi (Philips Research, NL)*	Library Suite 1	
11:00 h	Low Cost Launch-on-Shift Delay Test with Slow Scan Enable Signals *G. Xu, A. Singh (Auburn Univ., US)*		
11:30 h	Dynamic Voltage Scaling Aware Delay Fault Testing *N.B. Zain Ali, M. Zwolinski, B.M. Al-Hashimi (Univ. of Southampton, UK), P. Harrod (ARM, UK)*		
12:00 h	Enhancing Delay Fault Coverage through Low Power Segmented Scan *S. Reddy, Z. Zhang (Univ. of Iowa, US), J. Rajski (Mentor Graphics, US), B.M. Al-Hashimi (Univ. of Southampton, UK)*		

11:00-12:30	**Session 3B: Single-Event Upsets** *Moderators: B. Becker (Univ. Freiburg, DE)* *M. Sachdev (Univ. of Waterloo, CAN)*	Library Suite 2	
11:00 h	Single-Event Upset Analysis and Protection in High Speed Circuits *M. Hosseinabady, P. Lotfi-Kamran (Univ. of Tehran, IR), G. Di Natale, S. Di Carlo, A. Benso, P. Prinetto (Politecnico di Torino, IT)*		
11:30 h	Soft Error Resilient Linear DSM Systems: Probabilistic Error Correction vs. State Restoration *M. Ashouei, S. Bhattacharya, A. Chatterjee (Georgia Inst. of Tech., US)*		
12:00 h	Avoiding Circuit Simulation for the Analysis of Single Event Transient Propagation in Combinational Circuits *C. Neves (Univ. Federal de Pelotas, BR), I. Ribeiro, E. Henes Neto, G. Wirth (UERGS, BR), F. Lima Kastensmidt (UFRGS, BR), J.L. Güntzel (UFPEL, BR)*		

11:00-12:30	**Vendor Session 3C: Getting More Out of Test** *Moderators: G. Francis (Philips Semiconductors, UK)* *H. Lang (Freescale Semiconductor, DE)*	Garden Suite	
11:00 h	Test Management Systems - A New Category in the Testing Arena *D. Glotter (OptimalTest, Israel)*		
11:30 h	The Growing Impact of Manufacturing Test - Enabling DPM Reduction and Yield Learning *J. Rajski, B. Watt (Mentor Graphics, US)*		
12:00 h	Visibility Enhancement for Silicon Debug *Y.-C. Hsu, R. Ruiz (Novas Software, US)*		

12:30-14:00: Lunch

14:00-15:30	**Session 4A: Memory Testing - 1** *Moderators: C. Hill (Mentor Graphics, UK)* *E. Volkerink (Agilent Technologies, US)*	Library Suite 1	
14:00 h	Minimal March Tests for Dynamic Faults in Random Access Memories *G. Harutunyan, V. Vardanian (Virage Logic, Armenia), Y. Zorian (Virage Logic, US)*		
14:30 h	A 22n March Test for Realistic Static Linked Faults in SRAMs *A. Benso, A. Bosio, S. Di Carlo, G. Di Natale, P. Prinetto (Politecnico di Torino, IT)*		
15:00 h	Testing Active Neighborhood Pattern-Sensitive Faults of Ternary Content Addressable Memories *Y.-J. Huang, J.-F. Li (National Central Univ., TW)*		

14:00-15:30	**Session 4B: Test of Reconfigurable Systems** *Moderators: E. Larsson (Linköpings Univ., SE)* *B. West (Credence Systems, US)*	Library Suite 2	
14:00 h	Fault Identification in Reconfigurable Carry Lookahead Adder Implementations Targeting Nanoelectronic Fabrics *W. Rao, A. Orailoglu (UCSD, US), R. Karri (Polytechnic Univ., US)*		
14:30 h	Built-In Self-Test for PEs of Coarse Grained Dynamically Reconfigurable Devices *K. Katoh, H. Ito (Chiba Univ., JP)*		
15:00 h	Fault Injection-based Reliability Evaluation of SoPCs *M. Sonza Reorda, L. Sterpone, M. Violante (Politecnico di Torino, IT), M. Portela-Garcia, C. Lopez-Ongil, L. Entrena (Univ. Carlos III de Madrid, ES)*		

14:00-15:30	**Vendor Session 4C: At-Speed Test and Test Compression** *Moderators: M. Lousberg (Philips Research, NL)* *K. Thapar (Mentor Graphics, UK)*	Garden Suite	
14:00 h	Consideration of On-Chip Compression Alternatives *B. Keller (Cadence Design Systems, US), R. Illman (Cadence Design Systems, UK))*		
14:30 h	Keeping Test Simple *N. Mittermaier (Synopsys, DE)*		
15:00 h	Facilitating At-Speed Test at the Register Transfer Level *S. Swaminathan (Qualcomm, US), R. Marlett (Atrenta, US)*		

15:30-16:30	**Session 5: Student Forum Posters and Coffee/Tea Break**	**Avon**	
	Modeling and Automatic Test Pattern Generation for Mixed-Signal Boards in Maintenance Testing: Dealing With Simple Time Aspects *B. Gilles (Univ. de Bretagne Occidentale, FR)*		
	Accurate IDD Testing of Mixed-Signal Integrated Circuits using Auto-Zero Voltage Comparator *V. Nagy, V. Stopjaková (Slovak Univ. of Tech., Slovakia)*		
	HW Implementation of the Backtrace Algorithm *M. Št'áva, O. Novák (Czech Tech. Univ., CZ)*		
	Small Delay Defect Detection in the Presence of Process Variations		

	R. Tayade, S. Sundareswaran, J. Abraham (Univ. of Texas-Austin, US)		
	Connectionless Testing *M. Salamati, D. Stranneby (Őrebro Univ., SE)*		
	STESOC: A Software-Based Test-Access-Mechanism Controller M. Tuna, M. Benabdenbi, A. Greiner (Univ. of Paris VI, FR)		
	An Efficient Online BIST Architecture for NoCs *M. Hosseinabady, M. Nazm Bojnordi, A. Banaiyan, Z. Navabi (Univ. of Tehran, IR)*		

16:30-17:30	**Session 6A: Memory Testing - 2** *Moderators: S. Hamdioui (Delft Univ. of Tech., NL)* *P. Hughes (ARM, UK)*	Library Suite 1	
16:30 h	Retention-Aware Test Scheduling for BISTed Embedded SRAMs *Qiang Xu (Chinese Univ. of Hong Kong, HK), B. Wang (ATI Technologies, CAN), F.Y. Young (Chinese Univ. of Hong Kong, HK)*		
17:00 h	A Transparent-Based Programmable Memory BIST *S. Boutobza (Synopsys, FR), M. Nicolaidis (TIMA Laboratory, FR)*		

16:30-17:30	**Session 6B: Test and Measurement** *Moderator: G. Russell (Univ. of Newcastle-upon-Tyne, UK)* *Y. Zorian (Virage Logic, US)*	Library Suite 2	
16:30 h	A Flexible and Scalable Methodology for Testing High Speed Source Synchronous Interfaces on ATE with Multiple Fixed Phase Capture and Compare *B. Laquai, M. Hua, G. Schulze, M. Braun (Agilent Technologies, DE)*		
17:00 h	On-Chip Time Measurement Architecture with Femtosecond Timing Resolution *M. Collins, B.M. Al-Hashimi (Univ. of Southampton, UK)*		

16:30-17:30	**Vendor Session 6C: Jitter Test** *Moderators: J.-L. Carbonero (ST Microelectronics, FR)* *J. Rivoir (Agilent Technologies, DE)*	Garden Suite	
16:30 h credence	Moving Jitter Injection for High-Speed Digital Streams from the Analog Domain to the Digital Domain *R. Whyte (Credence, UK)*		
17:00 h Agilent Technologies	High Throughput PLL Testing – A Fast Method to Test Frequency and Jitter on Clock Outputs in Production *M. Braun, M. Fischer, J. Wolf (Agilent Technologies, DE)*		

17:30-19:00	**Panel Session 7A:** **Screening Is Only For Those Who Don't Know How To Test Better** *Organizers: E.J. Marinissen (Philips Research, NL), A. Singh (Auburn Univ., US)* *Moderator: E.J. Marinissen (Philips Research, NL)*	Library Suite 1	
	Screening is rejecting chips that pass all tests, but are suspect of being test escapes or latent reliability problems. Screening can for example be done on wafer neighborhoods (a die with too many failing dies as neighbors is suspect) or on parametric outlier measurements (a die with measurement values within spec, but sufficiently different from other passing dies). This panel session will discuss screening and its implications. What hardware and software infrastructure is necessary to enable screening? How effective is screening, and how is that measured? How expensive is screening; aren't we simply throwing away good dies? How does screening relate to burn-in? And, shouldn't we be improving our tests themselves? Panelists: • Tom S. Barnett (IBM Microelectronics, US) • Dan Glotter (OptimalTest, Israel) • Tim Daniels (LSI Logic, UK) • Adit Singh (Auburn University, US) • Co van Winsum (Philips Semiconductors, NL)		

17:30-19:00	**Panel Session 7B:** **How Relevant is Your Academic Preparation to Your Current Job Function?** *Organizers: E. Larsson (Linköpings Univ., SE),* *N. Nicolici (McMaster Univ., CAN)* *Moderator: M. Sonza Reorda (Politecnico di Torino, IT)*	Library Suite 2
	Universities strive to define appealing curricula to attract and educate top students and perform research that will impact long term industry needs. Employers look for skillful employees who can tackle the problems that require immediate solutions and who also have the depth to foresee the challenges of tomorrow. Given both the common interests and cultural differences between academia and industry, the question is how can we further improve the academic preparation to better serve the (test) industry in the long run? Join recent university graduates who will share their experience in transitioning from student to profession. Panelists: • Zaid Al-Ars (Delft Univ. of Tech., NL) • Thomas Clouqueur (AMD, US – ex Univ. of Wisconsin-Madison, US) • Artur Jutman (Tallinn Univ. of Tech, EST) • Martin Keim (Mentor Graphics, US – ex Univ. of Freiburg, DE) • Krishna Chakravadhanula (Cadence, US – ex Univ. of Texas-Austin, US) • Ross Torkington (ARM, UK – ex Sheffield Univ., UK) • Erik Volkerink (Agilent Technologies, US – ex Stanford Univ., US)	

17:30-19:00	**Panel Session 7C:** **EDA Test Synthesis, ATE Test Application – The Next Big Challenges?** *Organizer: B. Bennetts (Bennetts Associates, UK)* *Moderator: R. Marlett (Atrenta, UK)*	Garden Suite
	The EDA vendors have risen to the challenges of improved test-synthesis tools for at-speed test, test-data compression, and repairable memories. The ATE vendors have improved the capabilities of semiconductor testers in terms of measurements on high-speed buses: jitter injection and analysis, bit-error rate assessment, etc. So, what's next? What will be the major challenges of the test-synthesis and test-application vendors over the next five years as we drive down into 65nm technologies? More of the same, or something radically different? Come listen to the experts foretelling the future. Panelists: • Rob Aitken (ARM, US) • Janusz Rajski (Mentor Graphics, US) • Jochen Rivoir (Agilent Technologies, DE) • Robert Ruiz (Novas, US) • Mike Tegethoff (Cadence, US) • Steve Wigley (LTX, US) • Tom Williams (Synopsys, US)	

Tuesday May 23, 2006

08:30-10:00	**Session 8A: BIST and Test Data Compression for Logic** *Moderators: S. Hellebrand (Univ. of Paderborn, DE)* *Z. Peng (Linköpings Univ., SE)*	Library Suite 1	
08:30 h	On-Chip Test Generation Using Linear Subspaces *R. Das, I.L. Markov, J.P. Hayes (Univ. of Michigan, US)*		
09:00 h	Convolutional Compactors with Variable Polynomials *A. Pogiel (Poznań Univ., PL), J. Rajski (Mentor Graphics, US), J. Tyszer (Poznań Univ., PL)*		
09:30 h	Deterministic Logic BIST for Transition Fault Testing *V. Gherman, H.-J. Wunderlich (Univ. Stuttgart, DE), J. Schlöffel, M. Garbers (Philips Semiconductors, DE)*		

08:30-10:00	**Session 8B: Test of Sigma-Delta Modulators** *Moderator: S. Bernard (LIRMM, FR)* *A. Osseiran (Edith Cowan Univ., AUS)*	Library Suite 2	
08:30 h	Experimental Validation of a Fully Digital BIST for Cascaded SD Modulators *G. Leger, A. Rueda (Inst. de Microelectrónica de Sevilla, ES)*		
09:00 h	Evaluating Sigma-Delta Modulated Signals to Develop Fault-Tolerant Circuits *E. Schüler, D. Scain Farenzena, L. Carro (UFRGS, BR)*		
09:30 h	Bit Stream Manipulation for SD Modulator Failure Mode Detection *K. Georgopoulos, A. Lechner, A. Richardson, M. Burbidge (Lancaster Univ., UK)*		

08:30-10:00	**Vendor Session 8C: Memory and IDDQ Testing** *Moderators: J. Figueras (Univ. Polit. de Catalunya, ES)* *B. Kruseman (Philips Research, NL)*	Garden Suite	
08:30 h	Design for Yield with Embedded Tester for Memory Subsystem in SoC *L. Ternullo (Virage Logic, US)*		
09:00 h	Demystifying Repairable Memory *R. Aitken (ARM, US)*		
09:30 h	IDD(Q) Application to Analog and Mixed-Mode Circuits – A Case Study *S. Jing, A. Mathie, J. Garrison (National Semiconductor, US), H. Manhaeve (Q-Star Test, BE)*		

10:00-11:00	**Session 9: Posters and Coffee/Tea Break**	**Avon**	
	On-Line Testing of Digital Circuits for Non-Classical Fault Models: Resistive Bridging Fault Model and n-Detect Test *S. Biswas, S. Mukhopadhyay, A. Patra, D. Sarkar (IIT Kharagpur, IN)*		
	Outliers Screening with Multiple Parameter Correlation Testing for Analogue ICs *L. Fang, M. Lemnawar, Y. Xing (Philips Semiconductors, NL)*		
	Failure Mechanisms due to Process Variations in Nanoscale SRAM Core-Cells *P. Girard, S. Pravossoudovitch, A. Virazel (LIRMM, FR), M. Bastian (Infineon Technologies, FR)*		
	An Information-Redundant Scheme for On-Line Testing of an Asynchronous ALU Operation *M.J. Marshall, G. Russell (Univ. of Newcastle-upon-Tyne, UK)*		
	An Approach to Reduce Over-Testing of Path Delay Faults in Data Paths Using RT-Level Information *Y. Yoshikawa, S. Ohtake, H. Fujiwara (Nara Inst. of Science and Tech., JP)*		
	Detecting Hard-Faults Masked by Manufacturing Process Variations: a DAC Example *C. Wegener, M.P. Kennedy (Univ. College Cork, IRL)*		
	On the Use of Multi-Clock, Multi-VDD and Multi-Temperature Schemes to Improve Dynamic Fault Detection in Digital Systems *M. Rodriguez-Irago, J.J. Rodriguez Andina (Univ. of Vigo, ES), F. Vargas*		

	(PUCRS, BR), J. Semião (Univ. Algarve, PT), I.C. Teixeira, J.P. Teixeira (IST/INESC-ID, PT)		
	A Parallel Multilevel-Huffman Decompression Scheme for IP Cores with Multiple Scan Chains *X. Kavousianos (Univ. of Ioannina, GR), E. Kalligeros, D. Nikolos (Univ. of Patras, GR)*		
	Effects of Multiple Non-Concurrent Faults on Microprocessor Operation *E. Touloupis, J.A. Flint, V.A. Chouliaras (Loughborough Univ., UK), D.D. Ward (MIRA, UK)*		

11:00-12:30	**Session 10A: Current-Based and Power Switch Testing** *Moderators: P. Muhmenthaler (Infineon Technologies, DE)* *J.L. Huertas Diaz (CNM, ES)*	Library Suite 1	
11:00 h	Testing and Diagnosis of Power Switches in SOCs *S.K. Goel, M. Meijer, J. Pineda de Gyvez (Philips Research, NL)*		
11:30 h	A Robust 130nm-CMOS Built-In Current Sensor Dedicated to RF Applications *M. Cimino, H. Lapuyade, M. De Matos, T. Taris, Y. Deval, J.B. Bégueret (IXL Laboratory, FR)*		
12:00 h	Detecting Subtle IDDQ Faults by Using an Optimized Model-Based Estimator *J. Schat (Philips Semiconductors, DE)*		

11:00-12:30	**Session 10B: Test of AD and DA Circuits** *Moderators: A. Chatterjee (Georgia Inst. of Tech., US)* *A. Richardson (Univ. of Lancaster, UK)*	Library Suite 2	
11:00 h	"Analogue Network of Converters": A DFT Technique to Test a Complete set of ADCs and DACs Embedded in a Complex SiP or SOC *V. Kerzérho (LIRMM, FR), P. Cauvet (Philips Semiconductors, FR), S. Bernard, F. Azaïs, M. Comte, M. Renovell (LIRMM, FR)*		
11:30 h	Reducing Sampling Clock Jitter to Improve SNR Performance of A/D Converters in Production Test *S. Goyal, A. Chatterjee (Georgia Inst. of Tech., US), M. Atia (National Semiconductor, US)*		
12:00 h	Design-Based Structural Test Method for Stereo DAC *L. Ma, G. Seuren, R. van Rijsinge, C. Bastiaansen, L. van der Dussen (Philips Semiconductors, NL)*		

11:00-12:30	**Vendor Session 10C: Quality Cars, Quality Cell Phones, and Quality Research** *Moderators: R. Aitken (ARM, US)* *B. Bennetts (Bennetts Associates, UK)*	Garden Suite	
11:00 h	Improving Automotive IC Quality - A Case Study on the Implementation of Advanced IDDQ Strategies Targeting Product Quality Improvement, Burn-In Elimination and Test Cost Reduction *M. Schmid, R. Flassak, A. Patitz (Dialog Semiconductor, DE), H. Manhaeve (Q-Star Test, BE)*		
11:30 h	High-Efficiency Multi-Site Test for SiP Mobile Technologies *J. McEleney (Teradyne, US)*		
12:00 h	Involving Academia in Leading Edge Semiconductor Test Technology *P. Roddy (Advantest America, US)*		

12:30-14:00: Lunch

14:00-15:00	**Embedded Tutorial Session 11A** *Moderator: P. Harrod (ARM, UK)*	Library Suite 1	
14:00 h	Wafer Level Reliability Screens for Advanced CMOS *A. Singh (Auburn Univ., US)*		

14:00-15:00	**Embedded Tutorial Session 11B** *Moderator: T. Williams (Synopsys, US)*	Library Suite 2	
14:00 h	Soft-Error Rate Testing of Deep-Submicron ICs		

	T. Heijmen, A. Nieuwland (Philips Research, NL)		

14:00-15:00	**Embedded Tutorial Session 11C** *Moderator: N. Nicolici (McMaster Univ., CAN)*	Garden Suite	
14:00 h	New Techniques for Accessing Embedded Instrumentation: IEEE P1687 (IJTAG) *B. Eklow (Cisco Systems, US), B. Bennetts (Bennetts Associates, UK)*		

15:30-24:00: Social Event

Wednesday May 24, 2006

08:30-10:00	**Session 12A: Automatic Test Pattern Generation** *Moderators: S. Kajihara (Kyushu Inst. of Tech., JP)* *F. Pöhl (Infineon Technologies, DE)*	Library Suite 1	
08:30 h	Fault Collapsing for Transition Faults Using Extended Transition Faults *I. Pomeranz (Purdue Univ., US), S. Reddy (Univ. of Iowa, US)*		
09:00 h	FATE: a Functional ATPG to Traverse Unstabilized EFSMs *G. Di Guglielmo, F. Fummi, C. Marconcini, G. Pravadelli (Univ. di Verona, IT)*		
09:30 h	A Unified Method to Detect Transistor Stuck-Open Faults and Transition Delay Faults *N.B. Devta-Prasanna (Univ. of Iowa, US), A. Gunda, P. Krishnamurthy (LSI Logic, US), S. Reddy (Univ. of Iowa, US)*		

08:30-10:00	**Session 12B: Advanced Analog Testing** *Moderator: L. Carro (UFRGS, BR)* *M. Renovell (LIRMM, FR)*	Library Suite 2	
08:30 h	A Low-Cost Alternative Method for Harmonics Estimation in a BIST Context *V. Fresnaud, L. Bossuet, D. Dallet (Univ. of Bordeaux, FR), S. Bernard (LIRMM, FR), J.M. Janik (Univ. of Caen, FR), B. Agnus, P. Cauvet, Ph. Gandy (Philips Semiconductors, FR)*		
09:00 h	Optimized Signature-Based Statistical Alternate Test for Mixed-Signal Performance Parameters *B. Kim, H. Shin (Univ. of Texas-Austin, US), J.H. Chun (Intel, US), J. Abraham (Univ. of Texas-Austin, US)*		
09:30 h	Low-Cost Parametric Failure Diagnosis of RF Transceivers *D. Han, S. Bhattacharya, S. Goyal, A. Chatterjee (Georgia Inst. of Tech., US)*		

10:00-11:00	**Session 13: Posters and Coffee/Tea Break**	**Avon**	
	The Analysis of the Implementation of Concurrent Error Detection in Multi-Level Flash Memories *B. Halak, G. Russell (Univ. of Newcastle-upon-Tyne, UK)*		
	On-Chip Micro Programmable BIST for High SRAM Test Coverage *R. Zappa, C. Selva, D. Rimondi, C. Torelli (STMicroelectronics, IT)*		
	Diagnosis in Designs with Block Compactors *T. Clouqueur (Nara Inst. of Science and Tech., JP), K. Zarrineh (AMD, US), K.K. Saluja (Univ. of Wisconsin-Madison, US), H. Fujiwara (Nara Inst. of Science and Tech., JP)*		
	Estimation of RF IC Specifications Based on DC Tests *S. Ellouz, P. Gamand, C. Kelma (Philips Semiconductors, FR), B. Vandewiele (Philips Research, NL), B. Allard (Cegely Insa-Lyon, FR)*		
	Structural-Based Power-Aware Assignment of Don't Cares for Peak Power Reduction during Scan Testing *N. Badereddine, P. Girard, S. Pravossoudovitch, C. Landrault, A. Virazel (LIRMM, FR), H.-J. Wunderlich (Univ. Stuttgart, DE)*		
	A CAT Platform for Analogue and Mixed-Signal Test Evaluation and Optimization *A. Bounceur, S. Mir (TIMA Laboratory, FR), L. Rolíndez (ST Microelectronics, FR), E. Simeu (TIMA Laboratory, FR)*		
	Investigation of Single-Cell Dynamic Faults in Deep-Submicron Memory Technologies *S. Hamdioui, Z. Al-Ars, G.N. Gaydadjiev (Delft Univ. of Tech., NL), J.D. Reyes (Intel, US)*		
	Fault Tolerance Against SEUs using Memory-Based Circuits to Improve the Architecture Vulnerability Factor *E. Rhod, C. Lisbôa, A. Michels, L. Carro (UFRGS, BR)*		
	Stuck-At Fault Testing of FPGA Cores using Standard Test Pattern Generation		

	Tools *M. Bennebroek, H. Vranken, A. Danilin (Philips Research, NL)*		

11:00-12:30	**Session 14A: Test of Asynchronous and NOC Circuitry** *Moderators: K. Chakravadhanula (Cadence Design Systems, US)* *A. Yakovlev (Newcastle Univ., UK)*	Library Suite 1	
11:00 h	Wrapper Design for the Reuse of Networks-on-Chip as Test Access Mechanism *A. Amory (UFRGS, BR), K. Goossens, E.J. Marinissen (Philips Research, NL), M. Lubaszewski (UFRGS, BR), F. Moraes (PUCRS, BR)*		
11:30 h	A DFT Architecture for Asynchronous Networks-on-Chip *X.-T. Tran, J. Durupt, F. Bertrand (CEA-LETI, FR), C. Robach, V. Beroulle (INPG/ESISAR, FR)*		
12:00 h	Low-Cost Online Testing of Asynchronous Handshakes *D. Shang, A. Yakovlev, F. Burns, F. Xia, A. Bystrov (Univ. of Newcastle-upon-Tyne, UK)*		

11:00-12:30	**Session 14B: Diagnosis** *Moderators: H. Kerkhoff (Univ. Twente, NL)* *J.-P. Teixeira (IST/INESC-ID, PT)*	Library Suite 2	
11:00 h	Test-per-Clock Detection, Localization and Identification of Interconnect Faults *M. Kopec, T. Garbolino, K. Gucwa, A. Hławiczka (Silesian Univ. of Tech., PL)*		
11:30 h	On-Chip Evaluation, Compensation, and Storage of Scan Diagnosis Data - A Test Time Efficient Scan Diagnosis Architecture *F. Pöhl (Infineon Technologies, DE), J. Rzeha (Univ. of Potsdam, DE), M. Beck (Infineon Technologies, DE), M. Gössel (Univ. of Potsdam, DE), R. Arnold, P. Ossimitz (Infineon Technologies, DE)*		
12:00 h	CMOS Defects Analysis using DefSim Measurement Environment *W.A. Pleskacz, T. Borejko, A. Walkanis (Warsaw Univ. of Tech., PL), V. Stopjakova (Slovak Univ. of Tech., Slovakia), A. Jutman, R. Ubar (Tallinn Univ. of Tech., EST)*		

12:30-14:00: Lunch

14:00-15:30	**Session 15: Industrial Case Studies** *Moderators: L. Bouzaida (STMicroelectronics, FR)* *P. Varma (Blue Pearl Software, US)*	Library Suite 1	
14:00 h	Implementing the Gate Delay Test Method on a DECT Base-Band Design *J. ten Pierick (Philips Semiconductors, CH)*		
14:30 h	SiP Testing - An Industrial Case Study *H. Eichinger, G. Scheer (Infineon Technologies, AU)*		
15:00 h	An Industrial Approach to Re-order Integrated Circuit Tests to Maximize Test Benefit *S. Krishan, A. Zjajo (Philips Research, NL)*		

15:30: Closing Remarks and Introduction to ETS'07 by *B. Becker (Univ. of Freiburg, General Chair ETS'07)*
15:45: End of Symposium

= Submitted as Emerging Idea paper (review on 'novelty' only)

= Submitted as Case Study paper (review on 'results' only)

= Student Forum (NEW)

= Vendor Sessions (NEW)