Sunday May 21, 2006

09:00-17:00	**Full-Day Tutorials** *Organizer: Peter Harrod (ARM, UK) – ETS'06 Tutorial Chair* *Organized in cooperation with TTTC's Test Technology Educational Program (TTEP)*	Univ. of Southampton

Tutorial 1:
DFM, DFT, Silicon Debug and Diagnosis – The Loop to Ensure Product Yield
Presenters: Srikanth Venkataraman (Intel, US)
Nagesh Tamarapalli (Mentor Graphics, US)

Targeted Audience: Designers; test, DfT and product engineers; validation, yield, debug and failure analysis engineers; researchers; students and managers, and anyone who is interested in learning about state-of-the-art DfM, manufacturing test, debug and diagnosis methodologies that are being employed today across the industry.

Abstract: Semiconductor yield has traditionally been limited by random particle-defect based issues. However, as the feature sizes reduced to 0.18 µm and below, systematic mechanism-limited yield loss began to appear as a substantial component in yield loss due to the interaction between design and manufacturing. This tutorial covers the following topics. Design-for-Manufacturing (DFM) techniques to analyze the design content, flag areas of design that could limit yield, and make changes to improve yield. Test techniques to close the loop by crafting test patterns to expose the defect prone features during automatic test pattern generation (ATPG) and by analyzing silicon failures through diagnosis to determine the features that are actually causing yield loss and their relative impact. Design techniques (DFX) to improve testability, debuggability and diagnosability. Both basic concepts and theoretical aspects of debug and diagnosis are covered. The application of statistical diagnosis techniques to determine the features that are actually causing yield loss and their relative impact is presented.

Keywords: Design-for-Manufacturing, yield, feature-limited yield, DfM rule deck, reticle enhancement technology (RET), optical proximity correction (OPC), phase-shift masking (PSM), lithography, Design-for-Test (DfT), defects, defect-level, fault models, scan, ATPG, BIST, memory BIST, at-speed tests, DfM-oriented test, compressed test, silicon debug, diagnosis, scan chain diagnosis, logic diagnosis, at-speed diagnosis, high-volume statistical diagnosis, yield management systems.

Tutorial 2:
Delay-Fault Testing: From Basics to ASICs
Presenters: Ben Bennetts (Bennetts Associates, UK)
Bram Kruseman (Philips Research, NL)

Target Audience: Designers, test engineers and researchers interested in understanding and using delay-fault testing for the detection of defects.

Summary: At-speed testing of digital ICs using internal scan chains and targeted on propagation-delay faults is becoming a mainstream test method whose usage is no longer limited to high-speed ICs. Nowadays, it is a requirement for any IC manufactured in an advanced technology to obtain acceptable at-speed functional behaviour and manufacturing quality levels. This tutorial covers all aspects of at-speed testing for delay faults: starting with the basic causes of delay-fault failure mechanisms, and continuing with pattern generation and application protocols for at-speed test through scan chains, associated design-for-testability requirements, and implementation in a test program including meaningful analysis of the test responses. We will share industrial experiences as well as research directions to refine at-speed testing even further.

Keywords: Delay-fault test, hard and weak shorts and opens, fault models, ATPG, design-for-test, shmoo plots, delay mapping, clocking issues.