ETS'08 Fringe Workshop

Impact of Low Power Design on Test and Reliability

(LPonTR)

http://www.cad.polito.it/~ets08/

Grand Hotel Majestic, Pallanza, Lago Maggiore, Italy

Thursday, May, 29, 2008

Invited Talks:

- Kaushik Roy, Purdue Univ. (USA):
  "Power dissipation and process variation in Nanoscale CMOS design: test challenges and solutions"

- Bashir AlHashimi, Southampton Univ. (UK) and Peter Harrod, ARM (UK):
  "Impact of adaptive energy management on DFT"

- Sandip Kundu, Univ. Massachusetts at Amherst (USA):
  "Emerging trends in nanosilicone systems and their implications on design and test"

- Tobias Bjerregaard, CEO Teklatech (Denmark):
  "Timing variability and noise margins: will scaling kill the guardbands?"

- Enrico Macii, Politécnico di Torino (Italy):
  "Thermal aware design"

- Janusz Rajski, Mentor Graphics Corporation:
  "Power aware DFT"

- Tom Williams, Synopsis Inc.