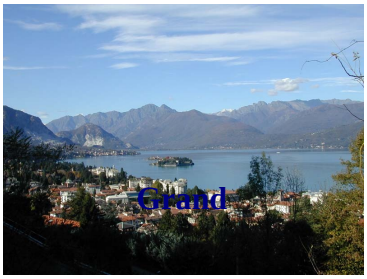

1st. International Workshop on the Impact of Low Power design on Test and Reliability (LPonTR)

Hotel Magestic, Pallanza, Lago Maggiore, Italy
Thursday, May, 29, 2008

LPonTR Programme

8:00 – 8:45	45m	Registration
8:45 – 9:00	15m	**Opening Remarks** (***J.P. Teixeira, Alex Bystrov***)
9:00 – 10:40	1h 40m	**Session 1 – Trends on LP Nano-silicon Systems and Power Management** (chair: Gert Jervan, Tallinn Univ., Estonia)

1.1. (Invited) ***Tom W. Williams***, Synopsys Fellow, USA, "Moore's/Dennard Law and Low Power Techniques"

1.2. (Invited) ***Sandip Kundu***, Univ. Massachusetts at Amherst, USA, "Emerging Trends in Nano-silicon Systems and their Implications on Design and Test"

1.3. (Invited) ***Bashir Al-Hashimi,*** Southampton Univ., ***Peter Harrod***, ARM, UK, "Impact of Adaptive Energy Management on DFT"

1.4. Introductory Short Presentations

1.4.a. ***Giorgio Di Natale, Marie-Lise Flottes, Bruno Rouzeyre***, LIRMM, F, "Stuck-at-Faults Test using Differential Power Analysis"

1.4.b. ***Satoshi Ohtake, Kewal K. Saluja***, Nara Institute of Science and Technology, JP, Univ. Wisconsin-Madison, USA, "A Systematic Scan Insertion Technique for Asynchronous On-chip Interconnects"

1.4.c. ***Michael E. Imhof, Hans-Joachim Wunderlich, Christian G. Zoellin***, Universitaet Stuttgart, Ge, "Integrating Scan Design and Soft Error Correction in Low-power Applications"

1.4.d. ***Bin Zhou, Yi-Zheng Ye, Zhao-lin Li***, Harbin Institute of Technology Harbin, China, "Reducing Test Storage, Time and Power Using Partial TRC-Reseeding and Scan Segments Freezing"

1.4.e. ***Chunhua Yao and Kewal K.Saluja***, University of Wisconsin-Madison, USA, "A Study of Word Oriented Random-Access-Scan Based BIST for Low Area Overhead and Low Power"

1.4.f. ***Fabian Vargas, Cláudia A. Rocha, Augusto Farina***, PUCRS, Porto Alegre, Brazil, "Power, Performance and Memory Overhead-Aware Checkpoint Insertion Based on Profiling Deployed Software"

1.4.g. ***Detlef Streitferdt, Philipp Nenninger, Holger Kaul, Florian Kantz,*** ABB AG, Corporate Research Center, Ge, "Low Power Development & Testing"

10:40 – 11:00	20m	**Coffee break + Poster session**

11:00 – 12:30 1h 30m **Session 2 – Thermal-aware Design and Variability**
(chair: Bernd Becker, Freiburg Univ., Ge)

2.1. (Invited) ***Enrico Macii***, Politecnico di Torino, Italy, "Thermal-aware Design: Problems, Challenges, Solutions"
2.2. ***S. Roy, B. Cheng, C. Millar, M. F. Bukhori, N. A. Kamsani, A. Asenov,*** University of Glasgow, Scotland, UK, "Intrinsic Timing Variability and Reliability of Nanoscale CMOS Circuits"
2.3. (Invited) ***Tobias Bjerregaard***, CEO Teklatech, Denmark, "Timing variability and noise margins: will scaling kill the guardbands?"
2.4. ***Domenik Helms, Marko Hoyer, Sven Rosinger, Wolfgang Nebel***, OFFIS Research Institute, Ge, "RT Level Makro Modelling of Leakage and Delay under Realistic PTV Variation"
2.5. Introductory Short Presentations
- 2.5.a. ***René Kothe***, Brandenburg Tech. University, Cottbus, Ge, "A Scan Controller Concept for Low Power Scan Test"
- 2.5.b. ***Ivano Midulla***, DeFacTo Technologies SA, F, "Test Power Estimation @RTL"
- 2.5.c. ***J. Freijedo, J. Semiao, J.J. Rodriguez-Andina, F.Vargas, I.C.Teixeira, J.P.Teixeira***, IST/TUL, P, Univ. of Vigo, Spain, "Delay Modeling for Power Noise-Aware Design and Test of Nanometer Digital Circuits"
- 2.5.d. ***Sudip Roy, Ajit Pal***, Indian Institute of Technology Kharagpur, India, "Transistor Sizing with Optimal-Vt for Runtime Leakage Reduction and LessSensitive Design under Leff Variations"

12:30 - 13:30 1h **Lunch**

13:30 – 14:00 30m **Interactive session** (posters / interactive / demos)
Design tools from *DeFacTo* and *Teklatech* demonstrated

14:00 - 15:45 1h 45m **Session 3 – Power-aware Design and Test: DFT and EDA**
(chair: Patrick Girard, LIRMM, F)

3.1. (Invited) ***Kaushik Roy***, Purdue Univ., USA, "Power Dissipation and Process Variation in Nanoscale CMOS Design: Test Challenges and Solutions"
3.2. (Invited) ***Janusz Rajski***, Mentor Graphics Corp., USA, "Power-aware DFT"
3.3. ***Irith Pomeranz***, Purdue Univ., USA, ***Sudhakar M. Reddy***, Univ. of Iowa, USA, "Functional Broadside Tests with Minimum and Maximum Switching Activity"
3.4. (Invited) ***Richard Illman,*** Cadence Design Systems, Inc., "ATPG Power Reduction Using Clock Gate "Default" Constraints"
3.5. ***J. Semião, J. Freijedo, J. Andina, F. Vargas, M. Santos, I. Teixeira, P. Teixeira***, IST/TUL, PUCRS, Brazil, P, Univ. Vigo, Spain, "Power and Time Management for Low-Power Design"

15:45 – 16:05 20m **Coffee Break**

16:05 – 16:50 45m **Session 4 – Panel: Challenges and Topics for Collaboration**
(moderator: ***K. Roy***)
Panelists: ***T. Bjerregaard, R. Illman , S. Kundu, J. Rajski***

16:50 – 17:00 10m **Closing Remarks** (***J.P. Teixeira, Alex Bystrov***)