ETS '08

European Test Symposium

FINAL PROGRAM

Grand Hotel Majestic
Verbania, ITALY
May 25-29, 2008

IEEE

IEEE COMPUTER SOCIETY

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Welcome

Foreword

On behalf of the Steering and Program Committees, we would like to welcome you to the European Test Symposium 2008 (ETS'08), the largest event in Europe that is entirely devoted to presenting and discussing trends, emerging results, hot topics, and practical applications in the area of electronic-based circuit and system testing. ETS'08 is the 13th edition of this symposium, and it is held in the Grand Hotel Majestic in Verbania on the Lago Maggiore (Italy).

ETS continues its well-established format with one day of tutorials, a three-day technical program, and an attractive social event. The symposium's technical program consists of two plenary keynote addresses, technical paper presentations in three parallel sessions, four embedded tutorials, poster sessions, two special sessions and two panels. Several test-related fringe events complete the "European Test Week," which includes the Workshop on Reliability & DfX Engineering for System-in-Package Technologies (SiPeX), the Workshop on Low Power Design Impact on Test and Reliability (LPonTR), a meeting organized by the Semiconductor Test Consortium (STC), and a Medea+ NanoTEST European project meeting.

ETS'08 received a large number of contributions from all over the world, submitted to the scientific track, workshop track (including emerging ideas and case studies), vendor sessions, and special sessions. All submissions underwent a rigorous review process. For the scientific and workshop tracks, each paper has been reviewed by no less than 6 reviewers. At a full-day TPC meeting, held on

to ETS 2008

February 1, 2008 at Montpellier, France, all papers were discussed and evaluated. Based on the reviews and the discussions, 27 scientific track papers were selected for inclusion in the ETS'08 Formal Proceedings. In addition, 9 workshop track papers were selected, alongside 18 vendor session presentations; most of these have corresponding papers in the ETS'08 Electronic Symposium Digest of Papers. Finally, 33 submissions were selected for poster presentations.

The European Test Symposium is the achievement of the contributions of many volunteers, who give generously their time to contribute to the success of the symposium. We would like to thank all for their efforts. We are confident that you will find ETS'08 a productive and exciting experience, and would like to welcome you to Verbania.

Matteo Sonza Reorda
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Patrick Girard
Program Chair

Zebo Peng
Program Vice-Chair

Christian Landrault
Cecilia Metra
Publication Co-Chairs

Presentations are marked as follows:

formal informal vendor

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M. Zwolinski – U. Southampton (UK)

The tutorials of ETS'08 are part of the annual IEEE Computer Society TTTC Test Technology Educational Program (TTEP) 2008.

The tutorials will take place on Sunday, May 25th, from 9:00 till 17:00. Tutorials will be held in the Hotel Il Chiostro, which is located about 3 km far from the Grand Hotel Majestic (where ETS is held).

9:00 – 17:00 TTEP Tutorial 1

DFx: The convergence of test, manufacturing, and yield

ROBERT AITKEN, *ARM Sunnyvale – USA*

Summary The tutorial goal is to show how design for yield (DFY) and design for manufacturability (DFM) are tightly coupled into what we conventionally think of as test, and that as process geometries shrink, the line between defects and process variation blurs to the point where it is essentially non-existent. In DFM/DFY circles, it is common to speak of defect limited yield, but it is less common to think of test-limited yield, yet this concept is common in DFT (e.g. IDDQ testing, delay testing). This tutorial will provide background needed for DFT practitioners to understand DFM and DFY, and see how their work relates to it. The ultimate goal is to spur attendees to conducting their own research in the area, and to apply these concepts in their jobs.

Intended Audience Test practitioners (engineers, students, academics) who are interested in learning more about the interaction between design and test, as they relate to yield, manufacturability and variability, and how they will affect chips in sub-90nm process technology.

Curriculum vitae *Robert C. Aitken* is an R&D Fellow at ARM. His areas of responsibility include design for testability and design for manufacturability. His research interests include defect analysis, fault diagnosis, and defect-based testing. He has given tutorials and short courses on several subjects at conferences and universities worldwide. He holds a Ph.D. degree from McGill University in Canada. Dr. Aitken is a senior member of the IEEE, and served as general chair of the 2005 International Test Conference.

9:00 – 17:00 TTEP Tutorial 2

IEEE 1500 - Building a Compliant Wrapper

Authors:
TERESA MCLAURIN, *ARM Austin – USA,*
TOM WAAYERS, *NXP Eindhoven – The Netherlands,*
FRANCISCO DA SILVA, *NVidia Santa Clara – USA.*

Presenters:
TERESA MCLAURIN and TOM WAAYERS.

Summary The purpose of this tutorial is to educate the audience with the challenges and benefits associated with implementing IEEE 1500 compliant wrappers for Core Test. This tutorial will also give an understanding of the reasons behind some of the rules in the standard. A 1500 wrapper, with CTL, is built piece by piece around an example bare core for illustration purposes. The pros and cons of different choices that are available to the user of the 1500 standard are discussed. All rules are discussed. Integration of cores and test scheduling in an SoC is also discussed.

Intended Audience This tutorial is for anyone who wants to understand the rules, the challenges and the benefits of IEEE 1500 core test wrapper standard and how it might be utilized to make test scheduling easier in an SoC.

Curriculum vitae *Teresa McLaurin*: The manager and technical lead of Test and DFT at ARM in Austin, TX. Prior to ARM, Teresa's work experience included DFT, as well as Product and Test Engineering. She contributed to the IEEE P1500 task force and lead the Instruction Tiger Team. She is a senior member of the IEEE and co-author of "The Core Test Wrapper Handbook: Rationale and Application of IEEE Std. 1500™".
Tom Waayers: Member of scientific staff and technical lead of DfT at Philips Research Laboratories in Eindhoven, The Netherlands. Tom's research interests include core-based design for test and debug methods. He is chair of Philips CTAG working group and was a member of the IEEE P1500 CTAG working group. He is co-author of "The Core Test Wrapper Handbook: Rationale and Application of IEEE Std. 1500™".
Francisco da Silva: Senior member of hardware design staff at NVIDIA Corporation. Prior to joining NVIDIA, held various positions at Synopsys Inc, including DFT methodology consulting and DFT tool development support positions. Also Editor-in-chief of the IEEE P1500 working group. He is co-author of "The Core Test Wrapper Handbook: Rationale and Application of IEEE Std. 1500™".

20:00 Welcome reception

The welcome reception will be held at the Grand Hotel Majestic.

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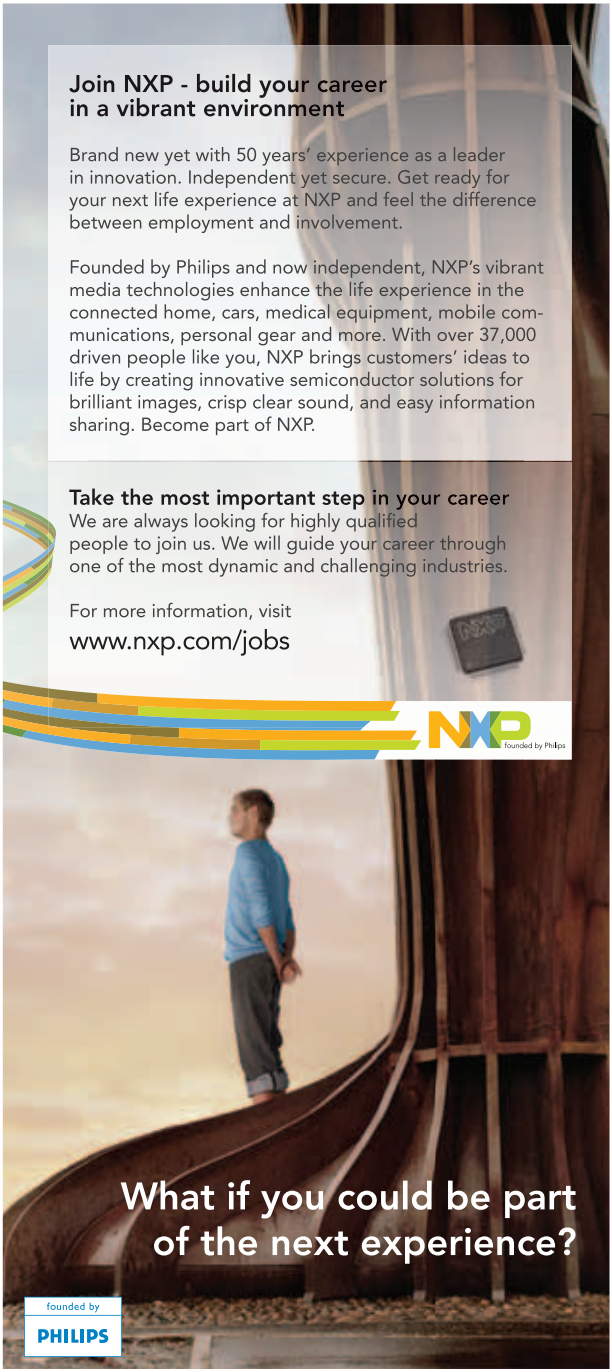

08:30 - 10:30 Session 1

Plenary Opening

Sala Toscanini

Moderator: Zebo PENG *Linköping University – Sweden*

8:30 - 9:10 Opening ceremony

Welcome Address
Matteo SONZA REORDA *Politecnico di Torino – Italy*, ETS'08 General Chair

Technical Program Introduction
Patrick GIRARD *LIRMM – France*, ETS'08 Program Chair

Presentation of ETS'07 Best Paper Award
Zebo PENG *Linköping University – Sweden*, ETS'07 Program Chair

TTTC Award Ceremony
Yervant ZORIAN, *Virage Logic - USA*, TTTC Senior Past Chair

9:10 - 9:50 Keynote 1

The Future Is Low Power and Test

T.W. WILLIAMS, *Synopsys – USA*

Curriculum Vitae Dr. *Thomas W. Williams* is a Synopsys Fellow at Synopsys in Boulder, Colorado, U.S.A. Formerly, he was with IBM Microelectronics Division and manager of the VLSI Design for Testability group. He received a B.S.E.E. from Clarkson University, an M.A. in pure mathematics from the State University of New York at Binghamton, and a Ph.D. in electrical engineering from Colorado State University. He has received numerous best paper awards from the IEEE and ACM, is the founder or co-founder of a number of workshops and conferences dealing with testing, and was twice a Distinguished Visitor lecturer for the IEEE Computer Society. Dr. Williams has previously served on the Computer Society Board of Governors and the IEEE Board of Directors, and was the Society's 2000 Treasurer. He is a member of the Eta Kappa Nu, Tau Beta Pi, IEEE, ACM, Sigma Xi, and Phi Kappa Phi. He is an Adjunct Professor at the University of Calgary, Calgary, Alberta, Canada; and in 1985 and 1997, he was a Guest Professor and Robert Bosch Fellow at the Universitaet of Hannover, Hannover, Germany. He was recently named a member of the Chinese Academy of Science. Dr. Williams was named an IEEE Fellow in 1988 and received the Computer Society's W. Wallace McDowell. Award for outstanding contributions to the computer art in 1989. In 2007 Dr. Williams received the European Design and Automation Association Lifetime Achievement Award for "outstanding contributions to the state of the art in electronic design, automation, and testing of electronic systems."

Abstract The talk will reconsider the role of the test in new emerging device circuits for CMOS Terascale and further technologies where a high level of redundancy will be present. As far as we are getting close to ultimate CMOS and ulterior new

emerging nano-devices technologies the indication made by J. von Neumann in 1950 that errors had to be viewed not as an extraneous accident but as an essential part of the process under consideration caused by natural phenomena is becoming a real fact. It is well accepted that at the same time electronic technology is going into the deep nanoscale the device reliability decreases rapidly. For such future technologies internal electromagnetic coupling or just thermal noise as well as permanent manufacturing defects will cause a loss of reliability and introduce an inherent error probabilistic factor to every component of the system. These deviations motivate new design paradigms. Many of these deviations will be transient in nature, at the same time current computer architecture approaches are reaching their practical limits. In order to build reliable electronics it will be necessary to include fault and defect tolerant schemes through the introduction of massive redundancy. Within this change of scenario, in comparison to conventional deterministic logic circuits these emerging technologies have to face new design and test strategies in order to give support to this probabilistic behaviour logic.

9:50 - 10:30 Keynote 2

The Role of Test in Circuits Built with Unreliable Components

Antonio RUBIO *Technical University of Catalonia (UPC) – Spain*

Curriculum Vitae *Antonio Rubio* received the M.S. and Ph.D. degrees from the Industrial Engineering Faculty of Barcelona, Spain. He has been Associate Professor of the Electronic Engineering Department at the Industrial Engineering Faculty, Technical University of Catalonia (UPC), Barcelona, and professor of the Physics Department at the Balearic Islands University, Spain. He is currently Professor of Electronic Technology at the Telecommunication Engineering Faculty in Barcelona. His research interests include VLSI design and test, nanoelectronics, device and circuit modelling, and high speed circuit design.

Abstract The talk will reconsider the role of the test in new emerging device circuits for CMOS Terascale and further technologies where a high level of redundancy will be present. As far as we are getting close to ultimate CMOS and ulterior new emerging nano-devices technologies the indication made by J. von Neumann in 1950 that errors had to be viewed not as an extraneous accident but as an essential part of the process under consideration caused by natural phenomena is becoming a real fact. It is well accepted that at the same time electronic technology is going into the deep nanoscale the device reliability decreases rapidly. For such future technologies internal electromagnetic coupling or just thermal noise as well as permanent manufacturing defects will cause a loss of reliability and introduce an inherent error probabilistic factor to every component of the system. These deviations motivate new design paradigms. Many of these deviations will be transient in nature, at the same time current computer architecture approaches are reaching their practical limits. In order to build reliable electronics it

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will be necessary to include fault and defect tolerant schemes through the introduction of massive redundancy. Within this change of scenario, in comparison to conventional deterministic logic circuits these emerging technologies have to face new design and test strategies in order to give support to this probabilistic behaviour logic.

11:00 - 12:30 Session 2A

Testing and Monitoring for High Quality Requirements

Sala Toscanini

Moderators: John P. HAYES *University of Michigan – USA*, Kewal SALUJA *University of Wisconsin-Madison – USA.*

Safe Fault Collapsing Based on Dominance Relations
IRITH POMERANZ *Purdue University – USA*, SUDHAKAR REDDY *University of Iowa – USA*

A Reliable Architecture for the Advanced Encryption Standard
GIORGIO DI NATALE *LIRMM – France*, MARION DOULCIER *LIRMM – France*, MARIE LISE FLOTTES *LIRMM – France*, BRUNO ROUZEYRE *LIRMM – France*

An Embedded Test & Health Monitoring Strategy for Detecting and Locating Faults in Aerospace Bus Systems
JARI HANNU *University of Oulu – Finland*, DENIS KOLTSOV *Lancaster University – United Kingdom*, ZHOU XU *Lancaster University – United Kingdom*, ANDREW RICHARDSON *Lancaster University – United Kingdom*, MARKKU MOILANEN *University of Oulu – Finland*

11:00 - 12:30 Session 2B

SoC Infrastructure

Sala Intra

Moderators: Jaan RAIK *Tallinn Technical University - Estonia*, Franc NOVAK *Jozef Stefan Institute - Slovenia.*

Bandwidth Analysis for Reusing Functional Interconnect as Test Access Mechanism
ARDY VAN DEN BERG *TU Delft – The Netherlands*, PENGWEI REN *TU Delft – The Netherlands*, ERIK JAN MARINISSEN *NXP Semiconductors – Netherlands*, GEORGI GAYDADJIEV *TU Delft – The Netherlands*, KEES GOOSSENS *NXP Semiconductors – The Netherlands.*

Analog Test Bus Infrastructure for RF/AMS Modules in Core–Based Design
VLADIMIR ZIVKOVIC *NXP Semiconductors – Netherlands*, FRANK VAN DER HEYDEN *NXP Semiconductors – Netherlands*,

JONG *NXP Semiconductors – Netherlands*, GUIDO GRONTHOUD *NXP Semiconductors – Netherlands.*

FPGA–based low–cost automatic test equipment for digital integrated circuits
LUCA MOSTARDINI *University of Pisa – Italy*, LUCA BACCIARELLI *University of Pisa – Italy*, LUCA FANUCCI *University of Pisa – Italy*, LORENZO BERTINI *SensorDynamics AG – Italy*, MARCO TONARELLI *SensorDynamics AG – Italy*, MARCO DE MARINIS *SensorDynamics AG – Italy.*

11:00 - 12:30 Vendor Session 2C

ATE Architectures

Sala Rotary

Moderators: Hans MANHAEVE *Qstar – Belgium*, Davide APPELLO *STMicroelectronics – Italy.*

A tester system architecture designed to fulfill the increasing test requirements of today's and future SoCs
ANDREE WEYH *Verigy – Germany.*

The mobile phone device test challenge
LUIGI CAZZANIGA *Teradyne – Italy.*

Aligning Academia With Leading Edge Semiconductor Test Technology
PAUL RODDY *Semiconductor Test Consortium – USA.*

14:00 - 15:30 Session 3A

Advances in RF Testing

Sala Toscanini

Moderators: Salvador MIR *TIMA – France*, Jose Luis HUERTAS DIAS *CNM – Spain.*

Confidence Estimation in Non-RF to RF Correlation-Based Specification Test Compaction
NATHAN KUPP *Yale University – USA*, PETROS DRINEAS *RPI – USA*, MUSTAPHA SLAMANI *IBM – USA*, YIORGOS MAKRIS *Yale University – USA.*

Built-in Test of Frequency Modulated RF Transmitters Using Embedded Low-Pass Filters
RAJARAJAN SENGUTTUVAN *Georgia Tech – USA*, ABHIJIT CHATTERJEE *Georgia Institute of Technology – USA*, HYUN CHOI *Georgia Institute of Technology – USA*, DONGHOON HAN *Georgia Institute of Technology – USA*.

Using temperature as observable of the frequency response of RF CMOS Amplifiers
JOSEP ALTET *Univ. Politecnica de Catalunya – Spain,*

EDUARDO ALDRETE–VIDRIO *Univ. Politecnica de Catalunya – Spain*, DIEGO MATEO *Univ. Politecnica de Catalunya – Spain*, ANTONIO RUBIO *Univ. Politecnica de Catalunya – Spain*, STEFAN DILHAIRE *Université Bordeaux I – France*, STEPHANE GRAUBY *Université Bordeaux I – France.*

14:00 - 15:30 Session 3B

Safe Test Generation and Design Validation

Sala Intra

Moderators: Bernd STRAUBE *Fraunhofer IIS/EAS Dresden – Germany*, Franco FUMMI *Univ. of Verona – Italy.*

A Capture-Safe Test Generation Scheme for At-Speed Scan Testing
XIAOQING WEN *Kyushu Institute of Technology – Japan*, KOHEI MIYASE *Kyushu Institute of Technology – Japan*, SEIJI KAJIHARA *Kyushu Institute of Technology – Japan*, HIROSHI FURUKAWA *Kyushu Institute of Technology – Japan*, YUTA YAMATO *Kyushu Institute of Technology – Japan*, KENJI NODA *Semiconductor Technology Academic Research Center – Japan*, HIDEAKI ITO *STARC – Japan*, KAZUMI HATAYAMA *Semiconductor Technology Academic Research Center – Japan,* TAKASHI AIKYO *Semiconductor Technology Academic Research Centor – Japan*, KEWAL SALUJA *Univ. of Wisconsin – Madison – USA.*

Temporally Extended High-Level Decision Diagrams for PSL Assertions Simulation
MAKSIM JENIHHIN *Tallinn University of Technology – Estonia*, JAAN RAIK *Tallinn Technical University – Estonia*, ANTON CHEPUROV *Tallinn University of Technology – Estonia,* RAIMUND UBAR *Tallinn Technical University – Estonia.*

On Bypassing Blocking Bugs during Post-Silicon Validation
EHAB ANIS DAOUD *McMaster University – Canada,* NICOLA NICOLICI *McMaster University – Canada.*

14:00 - 15:30 Vendor Session 3C

Parallel Testing

Sala Rotary

Moderators: Luigi CARRO *UFRGS – Brazil*, Anton CHICHKOV *AMIS – Belgium.*

New High Parallel RF Device Test Concep
KLAUS LUTZ *Advantest GmbH - Germany*, ADOLF FINKENZELLER *Advantest Europe – Germany.*

Innovative approach to Reliability and Test Solutions exploiting DfT on Low-cost Massively Parallel Testers
MASSIMILIANO GIANCARLINI *ELES Semiconductor Equipment – Italy*, ROGER CAGLIESI *ELES Semiconductor Equipment – Italy*, SANDRO GIORGI *ELES Semiconductor Equipment – Italy*, DOMENICO CHINDAMO *Independent Consultant – Italy.*

Very High parallelism Test Cell for Sensors
LUCIANO BONARIA *Spea – Italy.*

15:30 - 16:30 Session 4

Posters

Proactive diagnostics of solder interconnection failures with embedded precursor monitoring
JUHA VOUTILAINEN *University of Oulu – Finland*, JUSSI PUTAALA *University of Oulu – Finland*, MARKKU MOILANEN *University of Oulu – Finland*, HELI JANTUNEN *University of Oulu - Finland.*

Test Generation for Maximal Crosstalk Noise
MINJIN ZHANG *Institute of Computing Technology, Chinese Academy of Sciences – China,* HUAWEI LI *Chinese Academy of Sciences – China*, XIAOWEI LI *Chinese Academy of Sciences – China.*

Software-Based BIST Capabilities of the Advanced Encryption Standard
PAOLO MAISTRI *TIMA Laboratory – France*, REGIS LEVEUGLE *TIMA Laboratory - France*, CYRIL EXCOFFON *TIMA Laboratory – France.*

TTR+V: Triple Time Redundancy Plus Voting – A New Fault Masking Scheme for Multi-Context FPGAs
MARKUS HOLZ *Leibniz Universität Hannover – Germany,* ERICH BARKE *Leibniz Universität Hannover – Germany*

Exploiting Volume Diagnosis Data Filtering for Yield Learning
DAVIDE APPELLO *STMicroelectronics – Italy*, THOMAS WILLIAMS *Synopsys – USA*, EMIL GIZDARSKI *Synopsys – USA*, VINCENZO TANCORRE *STMicroelectronics – Italy*, PAUL TODARO *Synopsys – USA*, SALVATORE TALLUTO *Synopsys – USA*, GIUSEPPE DE NICOLAO *Università di Pavia – Italy*, PAOLO AMATO *STMicroelectronics – Italy.*

Advanced Digital Signal Inspector for the analysis of internal signals in pin-limited Systems-on-Package
LUCA BACCIARELLI *University of Pisa – Italy*, LUCA

MOSTARDINI *University of Pisa – Italy*, LUCA FANUCCI *University of Pisa – Italy*, CHRISTIAN ROSADINI *Sensor Dynamics AG – Italy*, ALESSANDRO ROCCHI *SensorDynamics AG – Italy*, MARCO DE MARINIS *SensorDynamics AG – Italy*, LUCA BENVENUTI *University of Pisa – Italy.*

A Novel Transient Fault Injection Method Based on STE Model Checking
ASHISH DARBARI *Southampton University – UK*, BASHIR AL-HASHIMI *Southampton University – UK*, PETER HARROD *ARM Ltd. – UK*, DARYL BRADLEY *ARM Ltd. – UK.*

Bidirectional Delay Test of FPGA Routing Networks
ELENA HAMMARI *NTNU – Norway*, MICHIKO INOUE *Nara Institute of Science and Technology – Japan*, EINAR J AAS *Norwegian University of Science and Technology (NTNU) – Norway*, HIDEO FUJIWARA *Nara Institute of Science and Technology – Japan.*

An Efficient Test and Characterization Approach for Nanowire-Based Architectures
EDUARDO RHOD *UFRGS – Brazil*, LUIGI CARRO *UFRGS – Brazil,* ERIKA COTA *UFRGS – Brazil.*

On Design of Hold Scan Cell for Hybrid Operation of a Circuit
HYUNBEAN YI *UMass - USA*, SANDIP KUNDU *University of Massachusetts - USA.*

The (Black) Art of Optimizing Test Vector Generation
HANS MANHAEVE *Q-Star Test – Belgium*, STEFAAN KERCKE-NAERE *Q-Star Test – Belgium*, GEIR EIDE *Magma Design Automation Inc. – USA*, JURAJ BRENKUS *STU-Bratislava – Slovakia.*

16:30 - 18:00 Session 5A

News from Memory Test

Sala Toscanini

Moderators: Said HAMDIOUI *TU Delft – The Netherlands,* Paul HUGUES *ARM Inc. – USA.*

Applying March Tests to K-Way Set-Associative Caches
STEFANO DI CARLO *Politecnico di Torino – Italy*, PAOLO PRINETTO *Politecnico di Torino – Italy*, ALESSANDRO SAVINO *Politecnico di Torino – Italy*, SIMONE ALPE *Politecnico di Torino – Italy.*

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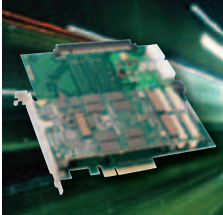
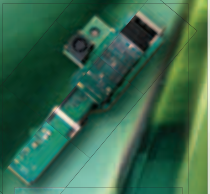


PCIe card-edge



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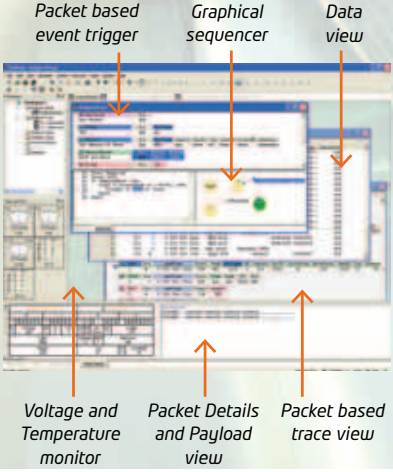
- Arrange trace data in Packet, Link, Split Transaction, Data or Lane Views with the click of a mouse
- Same GUI as the Vanguard PCI & VME analyzers
- Set up trigger events and sequences using drop down menus
- Extensive on-line help



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◆ **Hierarchical code correction and reliability management in embedded NOR flash memories**
BENOIT GODARD *Atmel Rousset – France*, JEAN MICHEL DAGA *Atmel Rousset – France*, LIONEL TORRES *LIRMM – France*, GILLES SASSATELLI *LIRMM – France.*

◆ **Self-Programmable Shared BIST for Testing Multiple Memories**
SWAPNIL BAHL *STMicroelectronics – India*, VISHAL SRIVASTAVA *STMicroelectronics – India.*

16:30 - 18:00 Session 5B

Diagnosis: New Concepts and Industrial Application

Sala Intra

Moderators: Helmut LANG *Freescale Semiconductor – Germany*, Bruno ROUZEYRE *LIRMM – France.*

◆ **Bridge Defect Diagnosis for Multiple-Voltage Design**
S. SAQIB KHURSHEED *University of Southampton – United Kingdom*, PAUL M ROSINGER *University of Southampton – United Kingdom*, BASHIR AL-HASHIMI *University of Southampton – United Kingdom*, SUDHAKAR REDDY *University of Iowa – USA*, PETER HARROD *ARM LTD – United Kingdom.*

◆ **Diagnose Multiple Stuck-at Scan Chain Faults**
YU HUANG *Mentor Graphics Corp. – USA*, WU-TUNG CHENG *Mentor Graphics Corp. – USA*, RUIFENG GUO *Mentor Graphics Corp. – USA.*

◆ **Increased Fault Diagnosis Throughput Using Dictionary for Hyperactive Faults**
CHEN LIU *University of Lowa – USA*, WU-TUNG CHENG *Mentor Graphics Corp. – USA,* HUAXING TANG *Mentor Graphics Corp. – USA,* SUDHAKAR REDDY *University of Lowa - USA*, WEI ZOU *Mentor Graphics Corp. – USA*, MANISH SHARMA *Mentor Graphics Corp. – USA*.

16:30 - 18:00 Vendor Session 5C

The Power of DfT

Sala Rotary

Moderators: Magdy ABADIR *Freescale – USA*, Carsten WEGENER *Infineon – Germany.*

◆ **Paving the way to 1000X compression**
GREG ALDRICH *Mentor Graphics Corp. – USA.*

Power - The new dimension of test
RICHARD ILLMAN *Cadence Designs Systems – USA*, MICHAEL O'SULLIVAN *Cadence Designs Systems – USA.*

Low Power Test Methodologies
NIKOLAUS MITTERMAIER *Synopsys GmbH – Germany.*

18:00 - 19:30 Panel Session 6A

Commercial tools for RTL Design-for-Test exist but how good are they?

Sala Toscanini

Organizer: Erik LARSSON, *Linköpings Universitet – Sweden*

Moderator: Nicola NICOLICI, *McMaster University – Canada.*

Abstract Design for Testability on RT-level descriptions has been extensively explored by academia as a research domain in the past decade, and now commercial tools are finally on the market, and start to be used in industrial design flows. The panel aims at gathering different opinions on these tools and on their future evolution: are they welcome from industry? How much are they effective? How well do they fit in the existing design flows? Which are the expectations for new techniques and tools? What is likely feasible, and what is simply a dream?

Panelists
CHOUKI AKTOUF *DeFacTo Technologies – France,*
WU-TUNG CHENG *Mentor Graphics Corp. – US,*
PRAB VARMA *BluePearl Software – USA,*
KEWAL SALUJA *University of Wisconsin-Madison – USA,*
MATTEO SONZA REORDA *Politecnico di Torino – Italy,*
SANDEEP GOEL *Magma Design Automation Inc. – USA.*

18:00 - 19:30 Panel Session 6B

No Beginners Beyond this Point

Sala Intra

Organizer: Erik Jan MARINISSEN *NXP Semiconductors – The Netherlands.*

Moderator: Adit SINGH *Auburn University – USA.*

Abstract Semiconductor process technologies continue to scale down, and hence become more sensitive for even the smallest disturbances. In addition, new transistor designs and the introduction of exotic new materials cause new, unfamiliar defect

modes. And as design complexity grows, there are more potential locations for failure. Despite all these trends, it seems that customers are only increasing their expectations with respect to product quality.
Design-for-Yield is a popular buzzword, but right now, test is still needed to help us meet these quality requirements. Can the test community keep up with the fast-forward mode of process technology and design? What is the best test approach now, and in the future, and does self-healing play a role in that? Will only companies that invest heavily in advanced test methods survive? Or is fault-tolerance our future?

Panelists
ROB AITKEN *ARM – USA,*
DAN GLOTTER *OptimalTest – ISRAEL,*
CARLO GUARDIANI *PDF Solutions – ITALY,*
PETER MUHMENTHALER *Infineon – GERMANY,*
KEITH ARNOLD *Pintail Technologies – USA.*

20:00 Dinner in pizzeria

Evening at pizzeria Bolongaro.

08:30-10:00 Session 7A

Delay Faults: Simulation, Test Generation and DFT

Sala Toscanini

Moderators: Seiji KAJIHARA *Kyushu Institute of Technology – Japan*, Arnaud VIRAZEL *LIRMM – France.*

◆ **A Simulator of Small-Delay Faults Caused by Resistive-Open Defects**
ALEJANDRO CZUTRO *University Freiburg – Germany*, NICOLAS HOUARCHE *LIRMM – France*, PIET ENGELKE *Albert Ludwigs University of Freiburg – Germany*, ILIA POLIAN *Albert Ludwigs University of Freiburg – Germany*, MARIANE COMTE *LIRMM Univ. of Montpellier – France*, MICHEL RENOVELL *LIRMM – France*, BERND BECKER *University of Freiburg – Germany.*

◆ **Critical Path Selection For Delay Test Considering Coupling Noise**
RAJESHWARY TAYADE *University of Texas – USA*, JACOB ABRAHAM *University of Texas – USA.*

◆ **Low Overhead Partial Enhanced Scan Technique for Compact and High Fault Coverage Transition Delay Test Patterns**
SEONGMOON WANG *NEC Labs America – USA*, WENLONG WEI *NEC Labs America – USA.*

08:30-10:00 Session 7B

SoC Testing

Sala Intra

Moderators: Sandeep K. GOEL *Magma Design Automation – USA*, Mounir BENABDENBI *LIP6 – France.*

◆ **Accelerated Shift Registers for X-tolerant test data compaction**
MARTIN HILSCHER *University of Potsdam – Germany*, MICHAEL BRAUN *VERIGY – Germany*, MICHAEL GOESSEL *University of Potsdam – Germany*, MICHAEL RICHTER *University of Potsdam – Germany*, ANDREAS LEININGER *Infineon Technologies AG – Germany.*

◆ **A new description language for SoC testing**
MICHELE PORTOLAN *Alcatel-Lucent Bell Labs – Ireland*, SURESH GOYAL *Alcatel-Lucent Bell Labs – USA*, BRADFORD G. VAN TREUREN *Lucent Technologies – USA*, CHEN-HUAN CHIANG *Lucent Technologies – USA*, TAPAN CHAKRABORTY

Alcatel-Lucent Bell Labs – USA, TOM COOK *Alcatel-Lucent Bell Labs – USA.*

An Innovative and Low-Cost Industrial Flow for Reliability Characterization of SoCs
PAOLO BERNARDI *Politecnico di Torino – Italy*, MICHELANGELO GROSSO *Politecnico di Torino – Italy*, ROGER CAGLIESI *ELES Semiconductor Equipment – Italy*, MASSIMILIANO GIANCARLINI *ELES Semiconductor Equipment – Italy*, DAVIDE APPELLO *STMicroelectronics – Italy.*

08:30-10:00 Vendor Session 7C

Potpourri

Sala Rotary

Moderators: Erik Jan MARINISSEN *NXP Semiconductors – The Netherlands*, Ilia POLIAN *Albert Ludwigs University of Freiburg – Germany.*

Overcoming the PCI Express debugging nightmare
VINCENZO DI CIANNI *VSYSTEMS SRL – Italy.*

Current Test Application Perspective
HANS MANHAEVE *Q-Star Test nv – Belgium.*

The Role of Silicon Aware IP in Shortening Time-to-Volume
YERVANT ZORIAN *Virage Logic – USA*.

10:00-11:00 Session 8

Posters

A Multi-Tone Signal Generation Technique for Production Test
SADOK AOUINI *McGill University – Canada*, GORDON ROBERTS *McGill University – Canada.*

Robust Tests for Transition Faults with Long Propagation Paths Using Boolean Satisfiability
STEPHAN EGGERSGLÜß *University of Bremen – Germany*, DANIEL TILLE *University of Bremen – Germany*, ROLF DRECHSLER *University of Bremen – Germany.*

Implementation of linear histogram based ADC testing, a case study
PETER MRAK *Jozef Stefan Institute – Slovenia*, ANTON BIASIZZO *Jozef Stefan Institute – Slovenia*, FRANC NOVAK *Jozef Stefan Institute – Slovenia.*

Posters continued

SET-Factor: An Analysis and Design Tool to Reduce SET Sensitivity in Integrated Circuits
FERNANDA KASTENSMIDT *UFRGS – Brazil*, CRISTIANO LAZZARI *CEITEC – Brazil*, THIAGO ASSIS *UFRGS – Brazil*, RICARDO REIS *UFRGS – Brazil*, LORENA ANGHEL *TIMA Laboratory – France*, GILSON WIRTH *UFRGS – Brazil.*

Design Methodology of Analog/Mixed-Signal Circuits For Yield Enhancement
LUO PEI-WEN *Industrial Technology Research Institute – Taiwan*, CHEN JWU-E *National Central University – Taiwan*, WEY CHIN-LONG *National Central University – Taiwan*, LIANG HSING-CHUNG *Chang Gung University – Taiwan*, CHEN JI-JAN *SoC Technology Center Industrial Technology Research Institute – Taiwan*, CHENG LIANG-CHIA *SoC Technology Center Industrial Technology Research Institute – Taiwan.*

An efficient Diagnosis Methodology for analog blocks: Application to Current Reference Circuits
HASSEN AZIZA *L2MP – France*, JEAN MICHEL PORTAL *L2MP/Polytech – France*, OLIVIER GINEZ *L2MP – France*, EMMANUEL BERGERET *L2MP – France*.

Fault Models and Injection Strategies for a Reflective Simulation Platform
ANTONIO MIELE *Politecnico di Milano – Italy*, CRISTIANA BOLCHINI *Politecnico di Milano – Italy*, DONATELLA SCIUTO *Politecnico di Milano – Italy.*

Novel Analog DFT for Data Retention Fault and Weak Cell Detection for SRAM Memories
MOHAMED AZIMANE *NXP Semiconductors – The Netherlands*, BRAM KRUSEMAN *NXP Semiconductors – The Netherlands*, ANANTA MAJHI *NXP Semiconductors – The Netherlands*.

Identification of dynamic faults in interconnects by the use of polynomial algebra
MICHAL KOPEC *Silesian University of Technology – Poland*, TOMASZ GARBOLINO *Silesian University of Technology – Poland*, KRZYSZTOF GUCWA *Silesian University of Technology – Poland,* ANDRZEJ HLAWICZKA *Silesian University of Technology – Poland.*

An IEEE P1687 Instrument for the Concurrent Testing of IEEE 1500 Wrapped Cores
MICHAEL HIGGINS *University of Limerick – Ireland.*

11:00-12:30 Session 9A

On-Chip Resources for Mixed-Signal Devices

Sala Toscanini

Moderators: Yiorgos MAKRIS *Yale University – USA*, Abhijit CHATTERJEE *Georgia Tech. – USA.*

◆ **Utilizing On-Chip Resources for Testing Embedded Mixed-Signal Cores**
CARSTEN WEGENER *Infineon Technologies AG – Germany*, HEINZ MATTES *Infineon Technologies AG – Germany*, STEPHANE KIRMSER *Infineon Technologies AG – Germany,* FRANK DEMMERLE *Infineon Technologies AG – Germany*, SEBASTIAN SATTLER *Infineon Technologies AG – Germany.*

◆ **An Improved Algorithm to Identify the Test Stimulus in Histogram-Based A/D Converter Testing**
ESA KORHONEN *University of Oulu – Finland*, JUHA KOSTAMOVAARA *University of Oulu – Finland.*

◆ **On-chip generation of sine-wave signals for low cost functional test**
MIGUEL DOMINGUEZ *University of Extremadura – Spain,* JOSE LUIS AUSIN *University of Extremadura – Spain,* GUIDO TORELLI *University of Pavia – Italy*, JUAN DUQUE-CARRILLO *University of Extremadura – Spain.*

11:00-12:30 Special Session 9B

NASA Flatsats: Spacecraft Testbeds for Mission Success

Sala Intra

Organizer: Michael WRIGHT *NASA – USA.*

Moderator: Yervant ZORIAN *Virage Logic – USA.*

Speakers:
MICHAEL WRIGHT *NASA – USA,*
DAVID AMASON *NASA – USA,*
STEVEN THIBAULT *JHU/APL – USA,*
PETER HARVEY *UC Berkeley – USA.*

Abstract This special session will address electronics testbeds ("flatsats") that have been developed by NASA Goddard Space Flight Center (GSFC) for testing spacecraft avionics and software. Flatsats from a range of "in-house" flight projects will be discussed, representing past and current missions: Lunar Reconnaissance Orbiter (LRO), Solar Dynamics Observatory (SDO), Space Technology -5 (ST-5), and Microwave Anisotropy Probe (MAP). The session will consist of brief presentations on the flatsat concept and descriptions of each project, followed by a question-and-answer period. Topics to be presented include:

mission overview, purpose and requirements of the flatsat system, functional description, benefits to respective projects, and any lessons learned.

11:00-12:30 Vendor Session 9C

Test Engineering

Sala Rotary

Moderators: Sandip KUNDU *Univ. of Massachusetts Amherst – USA*, Wu-Tung CHENG *Mentor Graphics – USA.*

◆ **Effective DPPM improvement programs require test program qualification and post-probe data analysis**
FREDERIC TILHAC *Test Advantage, Inc. – France.*

◆ **Observability of production test**
MEIR GELLIS *TestInsight – Israel.*

◆ **What if you could... join NXP?**
WINSTON SARRUCCO *NXP Semiconductors – The Netherlands.*

14:00-15:00 Embedded Tutorial Session 10A

Post-Silicon Validation and Debug

Sala Toscanini

Moderator: Prab VARMA *BluePearl Software – USA.*

Speakers:
BART VERMEULEN *NXP Semiconductors – The Netherlands,*
NICOLA NICOLICI *McMaster University – Canada.*

Abstract Pre-silicon verification methods work with models of the design and are therefore limited by the inherent trade-off between their accuracy and the associated simulation time. Designs are sent to fabrication when the confidence level seems high enough; unfortunately, it still happens that functional and electrical design errors remain undetected in pre-silicon verification and slip through to prototype silicon. Errors that slip through require fixing as soon as possible once detected on the prototype. Hence, the pre-silicon verification transitions to post-silicon validation and debug upon return of first silicon samples from the factory. The continued need for more effective and efficient debugging methods and instruments is expected to drive innovative and new debug research over the forthcoming years. In this tutorial, we present the fundamentals of this field, as well as give an overview of some recent advances in debug research and development. Topics to be covered include functional/electrical design errors, run-stop debugging, real-time functional observability, embedded instrumentation, integrated logic analysis,

transaction-based debug, and integrated hardware/software debug. This tutorial is intended to stimulate people into starting research and development work in this exciting field.

14:00-15:00 Embedded Tutorial Session 10B

Update: the P1687 (IJTAG) Hardware Proposal for Efficient Embedded Instrument Access, Bandwidth, and Connectivity – the ABC's of Embedded Content

Sala Intra

Moderator: Rob AITKEN *ARM – USA.*

Speakers:
ALFRED CROUCH *Inovys – USA,*
JEFF REARICK *AMD – USA,*
KEN POSSE *AMD – USA.*

Abstract Modern ICs have achieved a level of complexity where simple ATE test is not enough to determine if the part was designed and manufactured correctly – and modern packaging such as known good die and stacked die severely complicate the embedded landscape. More and more ICs are including Functional configuration choices; Debug logic (DFD); Test logic (DFT); manufacturing process and environment monitors (DFM); and yield-analysis support logic (DFY) – these logics need to be accessed at wafer probe, at package test, at board test, and even in-system. In the past, this logic was usually targeted at only one use environment and with ad hoc consideration for access – today these logics must interact with each other and they require formal scheduling and cataloguing to enable access, configuration, and operation that will fit within engineering budgets, cost and time budgets, and test equipment resource budgets. This embedded tutorial will show the multiple defined instrument interfaces to meet the access needs of various instruments; the connection schemes that can be applied versus engineering budgets such as area, routing, power, and access efficiency; the proposed high-bandwidth data connections that will allow high data-volume, targeted instrument latency, and instrument-to-instrument communication; and how all of this falls within the operating arena of the 1149.1 JTAG TAP and TAP Controller.

25-29 May, 2008

Sunday 25th

9:00-17:00 (at the hotel Il Chiostro)	**Tutorial 1** DFx: The convergence of test, manufacturing, and yield	**Tutorial 2** IEEE 1500 - Building a Compliant Wrapper
20:00	**Welcome reception at Grand Hotel Majestic with lakeside Italian flavors buffet**	

Monday 26th

8:30-10:30	**ETS'08 Plenary Opening**		
11:00-12:30	**Session 2A** Testing and Monitoring for High Quality Requirements	**Session 2B** SoC Infrastructure	**Session 2C** Vendor ATE Architectures
12:30-14:00	**Lunch**		
14:00-15:30	**Session 3A** Advances in RF Testing	**Session 3B** Safe Test Generation and Design Validation	**Session 3C** Vendor Parallel Testing
15:30-16:30	**Session 4 - Posters**		
16:30-18:00	**Session 5A** News from Memory Test	**Session 5B** Diagnosis: New Concepts and Industrial Application	**Session 5C** Vendor The Power of DfT
18:00-19:30	**Session 6A - Panel 1** Commercial tools for RTL Design-for-Test exist but how good are they?	**Session 6B - Panel 2** No Beginners Beyond this Point	
20:00	**Dinner in Pizzeria**		

ETS '08 - Program at-a-glance

Tuesday 27th

8:30-10:00	**Session7A** Delay Faults: Simulation, Test Generation and DFT	**Session 7B** SoC Testing	**Session 7C** Vendor Potpourri
10:00-11:00	**Session 8 - Posters**		
11:00-12:30	**Session 9A** On-Chip Resources for Mixed-Signal Devices	**Session 9B** Special Session 1 NASA Flatsats: Spacecraft Testbeds for Mission Success	**Session 9C** Vendor Test Engineering
12:30-14:00	**Lunch**		
14:00-15:30	**Session 10A** Embedded Tutorial 1 Post-Silicon Validation and Debug	**Session 10B** Embedded Tutorial 2 Update: the P1687 (IJTAG) Hardware Proposal for Efficient Embedded Instrument Access, Bandwidth, and Connectivity – the ABC's of Embedded Content	**Session 10C** Embedded Tutorial 3 DFT/BIST Circuit Techniques Using Sigma-Delta Encoding Methods
16:00	**Social Program**		

25-29 May, 2008
ETS '08 - Program at-a-glance

Wednesday 28th

8:30-10:00	**Session 11A** Solutions for Yield Enhancement	**Session 11B** Online Checking	**Session 11C** Vendor Design-for-Test
10:00-11:00	**Session 12 - Posters**		
11:00-12:30	**Session 13A** Embedded Tutorial 4		**Session 13B** Special Session 2
	Reliability, Availability and Serviceability of Networks-on-Chip		Collaborative Test Research in Europe
12:30-14:00	**Lunch**		
14:00-15:30	**Session 14** Soft Error Mitigation		
15:30-16:00	**ETS'08 Closing Session**		

Thursday 29th

	Fringe Workshops	
8:30-17:00	**Workshop on Reliability & DfX Engineering for System-in-Package Technologies - SiPeX**	**Workshop on Low Power Design Impact on Test and Reliability - LPonTR**

14:00-15:00 **Embedded Tutorial**
Session 10C

DFT/BIST Circuit Techniques Using Sigma-Delta Encoding Methods

Sala Rotary

Moderator: Adam OSSEIRAN *Edith Cowan University – Australia.*

Speaker:
GORDON ROBERTS *McGill University – Canada.*

Abstract This tutorial will look at different ways in which sigma-delta techniques can be used for DFT and BIST. One section will describe varous methods in which to generate high-precision analog signals, such as DC, sinusoids, multi-tones, Gaussian noise signals, phase and frequency modulated signals, etc. Such methods have application for retrofitting digital testers as mixed-signal testers, as well as extending the capability of existing mixed-signal testers. Subsequently, we'll demonstrate how sigma-delta methods can be used in a wide range of DFT/BIST circuits for SOC applications. This will include signal sources, digitizers, coherent samplers, time-domain reflectometry and transmission, and noise and jitter analyzers.

16:00 -23:00 **Social Event**

Lago Maggiore is one of the most charming places in Northern Italy, and the ETS'08 social event will let you taste the flavours of the history and the good life that mix together in the neighbourhood of Pallanza. Starting from Pallanza, we will cruise on the lake with the typical boats servicing visitors travelling on Lago Maggiore. The captains of our boats will guide us to the three of the most attractive places on the lake: hermitage of Santa Caterina del Sasso, Isola Bella, and Isola dei Pescatori.

The peculiar fascination of the hermitage of Santa Caterina del Sasso is due to the astonishing position on a rocky overhang, in one of the deepest points of the Lago Maggiore. The hermitage is formed by three different buildings dating from the XIII-XIV centuries. A legend tells that it was originated by a previous chapel dedicated to S. Caterina from Alessandria, which was erected in 1100 thanks to the intercession of the Saint herself by Alberto Besozzi of Arolo, a rich businessman who outlived from a downfall and therefore retired in that place as an eremite. Today the complex is made up of different buildings, juxtaposed in the gothic and Renaissance periods, linked through hanging balconies: the S. Caterina of Alessandria chapel, the church of S. Maria Nova, the church of S. Nicola (XIV C), the bell tower (XI C).

Isola Bella is one of the Borromean Islands of Lago Maggiore. Isola Bella is 320 meters long by 400 meters wide and is entirely occupied by the Palazzo Borromeo and its Italian garden. Until 1632 the island was occupied by a tiny fishing village: but that year Carlo III of the influential house of Borromeo began the construction of a palazzo dedicated to his wife, Isabella D'Adda, from whom the island takes its name.

The works continued for decades since then, and both the palace and the garden were finally inaugurated in 1671. The island achieved its highest level of social success during the period of Gilberto V Borromeo (1751 – 1837) when guests included Edward Gibbon, Napoleon and his wife Joséphine de Beauharnais, and Caroline of Brunswick, the Princess of Wales.

Isola dei Pescatori (Fishermen's Island) is the most northerly of the three principal Borromean Islands and, with a population of about 50, it is the only one to be inhabited all year round. Unlike Isola Bella and Isola Madre, the island no longer belongs to the Borromeo family. A narrow street running along its spine is joined by cobbled alleys to the promenade which encircles the island. The promenade is frequently flooded and the houses built against it are constructed to allow for this. While the traditional occupation of fishing still exists–local restaurants providing a ready market for the fish–tourism has become central to the economic life of the island as its picturesque charms have made Isola dei Pescatori a popular destination.
On the island we will enjoy a typical dinner at the Hotel Verbano. This small and romantic house will welcome us for a peaceful stay, rocked by the sweet atmosphere of the lake, plunged in a world that seems unreal, almost magic at the dusk, when the lapping of the waves of the lake is light and constant like an ancient lullaby.

8:30-10:00 Session 11A

Solutions for Yield Enhancement

Sala Toscanini

Moderators: Ahmad AL-YAMANI *King Fahd University of Petroleum and Minerals – Saudi Arabia*, Ricardo REIS *UFRGS – Brazil.*

Identifying Physical Root Causes for Yield Excursions from Test Fail Data
MANISH SHARMA *Mentor Graphics Corporation – USA*, BRADY BENWARE *Mentor Graphics Corporation – USA*, MARTIN KEIM *Mentor Graphics Corporation – USA*, HUAXING TANG *Mentor Graphics Corporation – USA,* I.Y. CHANG *UMC – Taiwan*, ALBERT MAN *AMD – Canada.*

When physical fault clustering meets pattern fault clustering
JAN SCHAT *NXP – Germany.*

Jitter Decomposition in High Speed Communication Systems
QINGQI DOU *University of Texas – USA*, JACOB ABRAHAM *University of Texas – USA.*

8:30-10:00 Session 11B

Online Checking

Sala Intra

Moderators: Lorena ANGHEL *TIMA – France*, Sandeep GUPTA *USC – USA.*

Risks for Signal Integrity in System in Package and Possible Remedies
DANIELE ROSSI *University of Bologna – Italy,* PAOLO ANGELINI *DEIS - University of Bologna – Italy,* CECILIA METRA *University of Bologna – Italy,* GIOVANNI CAMPARDO *STMicroelectronics – Italy*, GIAN PIETRO VANALLI *STMicroelectronics – Italy.*

Detecting Multi-cycle Errors using Invariance Information
NUNO ALVES *Brown University – USA*, KUNDAN NEPAL *Bucknell University – USA*, BRYANT MAIRS *Brown University – USA*, JENNIFER DWORAK *Brown University – USA*, IRIS BAHAR *Brown University - USA.*

◆ **Function Inherent Code Checking: A New Low Cost On-Line Testing Approach For High Performance Microprocessor Control Logic**
CECILIA METRA *University di Bologna – Italy*, DANIELE ROSSI *University of Bologna – Italy*, MARTIN EUGENIO OMANA *University of Bologna – Italy,* ABHIJIT JAS *Intel Corporation – USA,* RAJESH GALIVANCHE *Intel Corporation – USA.*

8:30-10:00 Vendor Session 11C

Design-for-Test

Sala Rotary

Moderators: Srikanth VENKATARAMAN *Intel – USA*, Ondrej NOVAK *Czech Technical Univ. – Czech Republic.*

◆ **Scan-Through-TAP: Combining Scan Chain and Boundary Scan Features in SOC**
ZORAN STAMENKOVIC *IHP – Germany*, MARY GILES *Synopsys Inc. – USA*, FRANCISCO RUSSI *Synopsys Inc. – USA.*

◆ **Inserting DFT at RTL Becomes Real**
CHOUKI AKTOUF *DeFacTo Technologies – France.*

◆ **Physical-Aware ATPG: What Does It Really Mean?**
SANDEEP GOEL *Magma Design Automation – USA*, GEIR EIDE *Magma Design Automation – USA*, ROBERT THOMPSON *Magma Design Automation – USA.*

10:00-11:00 Session 12

Posters

◆ **A Temperature and Power Supply Independent CMOS Voltage Reference for Built-In Self-Test**
LUCA TESTA *IMS Laboratory – France*, MIKAEL CIMINO *IXL Laboratory – France*, HERVE LAPUYADE *IXL Laboratory – France*, YANN DEVAL *IMS Laboratory – France*, JEAN-LOUIS CARBONERO *STMicroelectronics – France,* JEAN-BAPTISTE BEGUERET *IMS Laboratory – France.*

◆ **Improved Circuit-to-CNF Transformation for SAT-based ATPG**
DANIEL TILLE *University of Bremen – Germany*, RENE KRENZ-BAATH *NXP Semiconductors GmbH – Germany*, JUERGEN SCHLOEFFEL *Philips Semiconductors Gmbh – Germany,* ROLF DRECHSLER *University of Bremen – Germany.*

◆ **Design-for-Debug Architecture for Distributed Embedded Logic Analysis**
HO FAI KO *McMaster University – Canada,* ADAM KINSMAN

McMaster University – Canada, NICOLA NICOLICI *McMaster University – Canada.*

◆ **Timing Yield Modelling Based on Simulation of Lithography Process**
ASWIN SREEDHAR *University of Massachusetts – USA*, SANDIP KUNDU *University of Massachusetts – USA.*

◆ **Diagnosis of Multiple Scan Chain Failures**
NADIR BASTURKMEN *Intel – USA*, RUIFENG GUO *Mentor Graphics Corp. – USA,* SRIKANTH VENKATARAMAN *Intel Corporation – USA.*

◆ **SystemC-based Fault Injection Technique with Improved Fault Representation**
RISHAD SHAFIK *University of Southampton – UK,* PAUL M ROSINGER *University of Southampton – UK,* BASHIR AL-HASHIMI *University of Southampton – UK.*

◆ **Efficient scheduling of delay tests for latch-based circuits**
KUN YOUNG CHUNG *University of Southern California – USA,* SANDEEP GUPTA *University of Southern California – USA.*

◆ **Shrinking the Application Time of Test Set Embedding by Using Variable-State Skip LFSRs**

VASILIOS TENENTES *University of Ioannina – Greece,* KAVOUSIANOS CHRISOVALANTIS *University of Ioannina – Greece,* EMMANOUIL KALLIGEROS *University of Patras – Greece.*

11:00-12:30 Embedded Tutorial Session 13A

Reliability, Availability and Serviceability of Networks-on-Chip

Sala Toscanini

Moderator: Gert JERVAN *Tallinn University of Technology – Estonia.*

Speakers:
ERIKA COTA *UFRGS – Brazil*,
MARCELO LUBASZEWSKI *UFRGS – Brazil.*

Abstract This tutorial presents an overview of the issues related to the test, diagnosis and fault-tolerance of NoC-based systems. First, the characteristics of the NoC design (topologies, structures, routers, wrappers, and protocols) are presented, as well as a summary of the terms used in the field and an overview of the existing industrial NoCs is given. Then, the

challenges to test, diagnose and tolerate faults in a NoC-based system are discussed. Current test strategies are then presented: re-use of on-chip network for core testing, test scheduling for the NoC reuse, test access methods and interface, efficient re-use of the network, and power-aware and thermal-aware testing. In addition, the challenges and solutions for the NoC (interconnects, routers, and network interface) test and diagnosis are presented. Finally, since quality-of-service is one of the main challenges for the NoC use, fault tolerance techniques

11:00-12:30 Special Session 13B

Collaborative Test Research in Europe

Sala Intra

Organizer: Hans-Joachim WUNDERLICH *Universität Stuttgart – Germany.*

Moderator: Hans-Joachim WUNDERLICH *Universität Stuttgart – Germany.*

Speakers:
KEES VEELENTURF *Nanotest, NXP – The Netherlands,*
SYBILLE HELLEBRAND *Realtest, University of Paderborn – Germany,*
ANDREW RICHARDSON *NoE Patent-DfMM, University of Lancaster – UK,*
SEBASTIAN SATTLER *Maya, Infineon – Germany,*
PETER MUHMENTHALER *Infineon – Germany,*
MICHEL BURLE *Medea Office – France,*
PAUL RODDY *ITRS Advantest – USA.*

Abstract Representatives of large national and international joint research projects in the area of test will share their experiences. The benefits and the technical results, the added value of joint research and the organisation and administration of large projects as well as the presentation and evaluation of the research results will be discussed. Furthermore, topics and possibilities of future joint projects will be investigated under both technical and organizational aspects.

14:00-15:30 Session 14

Soft Error Mitigation

Sala Toscanini

Moderators: Matthias PFLANZ *IBM – Germany*, Virendra SINGH *IISc Bangalore – India.*

◆ **Selective Hardening in Early Design Steps**
CHRISTIAN ZOELLIN *Universität Stuttgart – Germany,* HANS-JOACHIM WUNDERLICH *Universität Stuttgart – Germany,* ILIA POLIAN *Albert Ludwigs University of Freiburg – Germany*, BERND BECKER *University of Freiburg – Germany.*

◆ **Tunable transient filters for soft error rate reduction in combinational circuits**
QUMING ZHOU *Rice University – USA*, MIHIR CHOUDHURY *Rice University – USA*, KARTIK MOHANRAM *Rice University – USA.*

◆ **Convolutional coding for SEU mitigation**
LAURA FRIGERIO *Politecnico di Milano – Italy*, MATTEO RADAELLI *Politecnico di Milano – Italy*, FABIO SALICE *Politecnico di Milano - Italy.*

15:30-16:00 Session 15

Closing Remarks and Introduction to ETS'09

Sala Toscanini

Closing Remarks:
Matteo SONZA REORDA
Politecnico di Torino – Italy
ETS'08 General Chair.

Introduction to ETS'09
Jose Luis HUERTAS DIAS
CNM Seville - Spain
ETS'09 General Chair.

Fringe Workshops

8:30 – 17:00

1st Workshop on Reliability & DfX Engineering for System-in-Package Technologies (SiPeX)

Chair: A. RICHARDSON *U. Lancaster – UK.*
Co-Chair: P. NOUET *LIRMM – France.*

The SiPeX workshop aims to bring together reliability and test engineers to discuss advanced design methodologies, integration technology and assembly engineering for SiP solutions that embrace heterogeneity, multiple energy domains and mixed technology platforms.

8:30 – 17:00

1st Workshop on Low Power Design Impact on Test and Reliability (LPonTR)

Chair: Alex BYSTROV *Newcastle University – UK.*
Co-Chair: J. Paulo TEIXEIRA *IST INESC-ID – Portugal.*

The LPonTR workshop aims to bring together design, reliability and test engineers and researchers to discuss the impact of advanced low-power / low voltage design methodologies of nanometer silicon systems on test and reliability. Power and thermal issues, leakage, process variations, enhanced susceptibility to environmental and operation-induced disturbances are physical constraints that drive the need to the development of low-power, process-tolerant design techniques. However, these techniques generate a new set of test and reliability challenges, questing for an innovative set of methodologies and tools.

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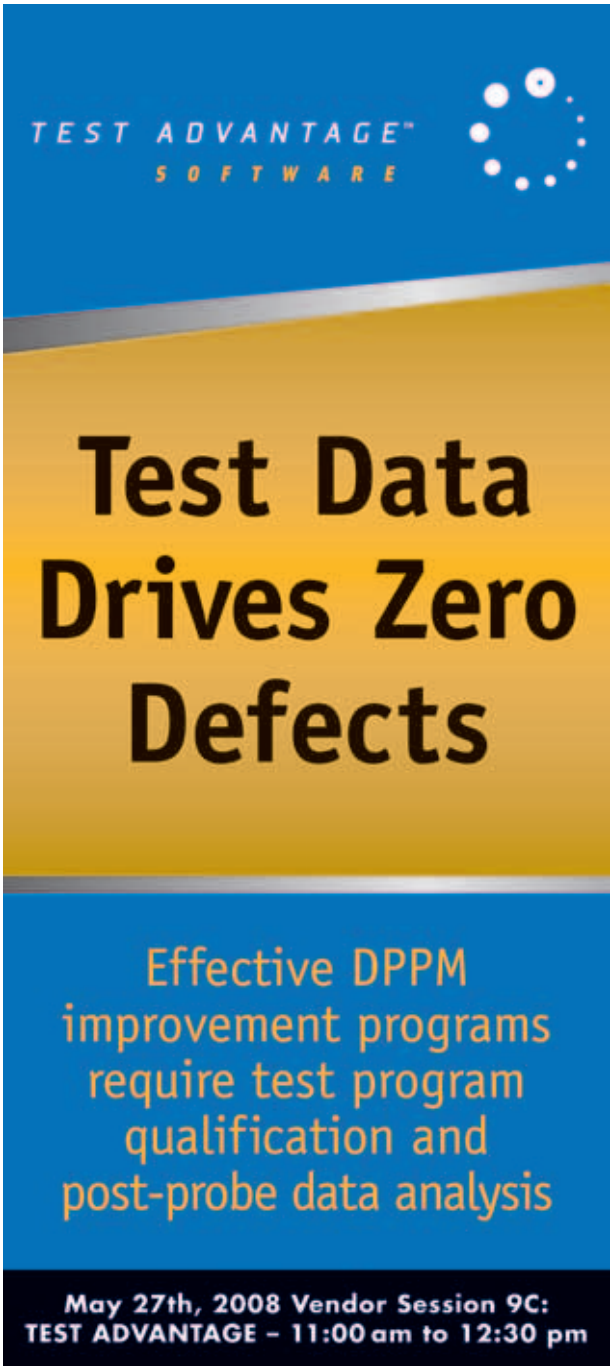
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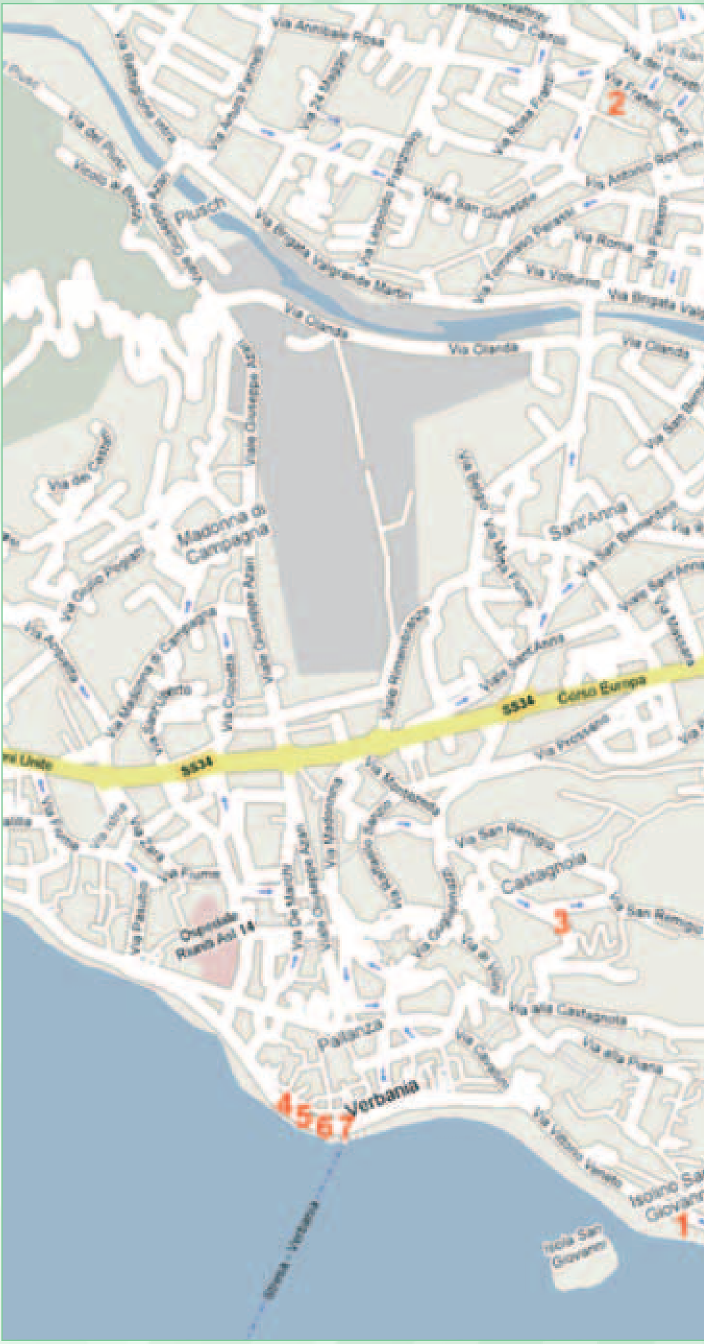

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