



3rd International Workshop on

# Impact of Low-Power design on Test and Reliability LPonTR'10

Prague, Czech Republic  
May 27-28, 2010

Fringe to 

<http://www.staff.ncl.ac.uk/a.bystrov/LPonTR/>

<http://ets2010.felk.cvut.cz>

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Alex Bystrov, Newcastle Univ., UK

Patrick Girard, LIRMM, France

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## Call for Papers

The International Workshop on *Impact of Low Power Design on Test and Reliability* (LPonTR) aims to bring together design, reliability and test engineers and researchers to discuss the impact of advanced low-power low-voltage design methodologies of nanometer silicon systems on test and reliability. Power and thermal issues, leakage, process variations, susceptibility to environmental and operation-induced interference are physical constraints that drive the development of low-power, process-tolerant design techniques. However, these techniques generate a new set of test and reliability challenges, questing for an innovative set of methodologies and tools.

You are invited to participate in LPonTR'10. Papers are invited that address current trends, challenges and proposed solutions in the following areas (but are not limited to):

- Power and process variations aware design and test
- Challenges of Ultra Low-power design on test and reliability
- Design for Variability and its effect on testing
- Reliability issues in silicon technologies below 45 nm
- Delay testing for high-performance low-power products
- Test and reliability implications of leakage
- Test, reliability and power consumption of physical on-chip infrastructures
- Dynamic BIST and Scan design for process tolerant LP products
- test of SoC with power and thermal management
- Test and reliability of highly dependable, redundant systems
- Low-power, low-voltage DfT
- Signal integrity in test mode
- Discriminating physical defects from noise and uncertainty
- Defect modelling, fault simulation and ATPG for emerging failure modes
- Analog, mixed-signal and asynchronous low-power design, test and DfT
- Statistical and parametric test
- EDA tools to support process-tolerant LP design

**Submissions** – The organising committee invites authors to submit **extended abstracts** in the above areas. All submissions will be peer-reviewed and accepted abstracts will be published in the informal proceedings of the workshop.

**Presentations** – A number of accepted papers will be chosen for a **full oral** presentation (15-20 min.) and, optionally, **tool demonstration**. The other accepted papers will be presented as a **short oral** (2 min.) in addition to either a **poster** or **interactive/demo** presentation.

**Journal Publications** – The best contributions will be invited for publication as a full paper in a special section on LPonTR'10 in the ASP Journal of Low Power Electronics (JOLPE) - <http://www.aspbs.com/jolpe/>. All accepted papers will be considered regardless of the form of presentation. In 2008-9 ten papers were accepted to JOLPE after the second round of reviewing.

**Formats** – *Format for the extended abstracts*: 2 pages, IEEE conference layout or latex8, font 10, two columns, paper A4, no page numbering, in PDF file format. Approximate dimensions: left/right margin 20mm, top/bottom margin 30mm, column separation 8mm, single line spacing.

*Format for posters*: up to A0-portrait. *Format for demonstrations*: please contact the chairs.

**Communication** – Please e-mail your manuscripts directly to [a.bystrov@ncl.ac.uk](mailto:a.bystrov@ncl.ac.uk)

### Key Dates:

- Submission deadline: **15th March, 2010**
- Notification of acceptance : 26th April, 2010
- Final manuscript (electronic format) : 10th May, 2010

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