Program

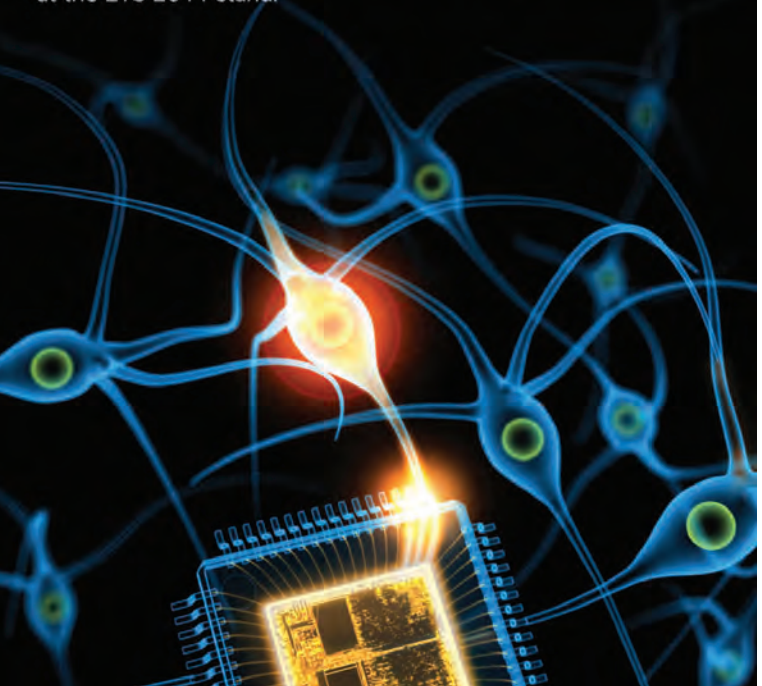
ETS 2011 | 16TH IEEE EUROPEAN TEST SYMPOSIUM | TRONDHEIM / NORWAY MAY 23RD-27TH

Sponsors

Welcome to ETS 2011

On behalf of the Steering and Program Committees, we would like to welcome you to the European Test Symposium 2011 (ETS'11), the largest event in Europe that is entirely devoted to presenting and discussing trends, emerging results, hot topics, and practical applications in the area of electronic-based circuit and system testing.

ETS'11 is the 16th edition of this symposium, and it is held in Trondheim, Norway. Situated in the middle of Norway, it is one of the oldest cities in Norway, with a thousand year history. ETS'11 continues its well-established format with a three-day technical program, and an attractive social event. The symposium's technical program consists of two plenary keynote addresses, technical paper presentations in three parallel sessions, two embedded tutorials, three poster sessions, two panels, and a special session featuring a student contest and student work-in-progress. Several test-related fringe events complete the "European Test Week," which includes the Workshop on Impact of Low Power Design on Test and Reliability (LPonTR'11), the Workshop on Processor Verification, Test and Debug (IWPVTD'11), and the Workshop on Low Power Design Impact on Test and Reliability (LPonTR) and the Test Spring School (TSS).



ETS'11 received a large number of contributions from all over the world, submitted to the scientific track, workshop track (including emerging ideas and case studies), vendor sessions, and special sessions. All submissions underwent a rigorous review process. For the scientific and workshop tracks, each paper has been reviewed on average by at least eight reviewers. At a full-day TPC meeting, held on February 4, 2011 in Linköping, Sweden, all papers were discussed and evaluated. Based on the reviews and the discussions, 32 scientific track papers, and 18 one page abstracts describing corresponding posters were selected for inclusion in the ETS'11 Formal Proceedings. This year for the second time there is an electronic version of proceedings only, each symposium participant will receive a flash memory with the proceedings. In addition, 10 contributions for the workshop track and 12 vendor session presentations were selected; most of these have corresponding papers in the informal part of the electronic proceedings.

The European Test Symposium is the achievement of the contributions of many volunteers, who give generously their time to contribute to the success of the symposium. We would like to thank all for their efforts.

We are confident that you will find ETS'11 a productive and exciting experience, and would like welcome you to Trondheim.

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General information

Organizers

Norwegian University of Science and Technology,Trondheim, Norway
Linköping University, Linköping, Sweden

Date / Symposium venue

May 23-27, 2011
Realfagbygget, Høgskoleringen 5, Gløshaugen, Trondheim, Norway

Registration / Information hours

REALFAGBYGGET	Monday May 23rd	13.00 - 15.00
BRITANNIA HOTEL	Monday May 23rd	18.00 - 19.00
REALFAGBYGGET	Tuesday May 24th	08.00 - 19.00
	Wednesday May 25th	08.00 - 15.00
	Thursday May 26th	08.00 - 15.00
	Friday May 27th	08.00 - 12.00

Board

Lunches will be served in the canteen at the premises.
Coffee breaks are given in the halls at the premises.

Practical Information

MONEY

Currency: Norwegian kroner (NOK) Rate: 1 EUR is about 8 NOK.
There is one ATM at the venue, and several down town.
All major credit cards are accepted in stores and restaurants.

PUBLIC TRANSPORT

Busses run between the city center and the venue every day.
Bus no. 52 is scheduled for every 15 minutes during the conference hours. Runs from Torvet and stops 2 minutes walk from the venue.
Tickets are sold on the bus.

We have organized a few busses every morning from the city to Realfagbygget. Schedules are found on the ETS'11 web site.

Photo: Jørn Adde © Trondheim kommune.

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Bjørn B. Larsen (NO)	Local Arrangements, Audio-visual, Web

Social events

Monday 23rd	Reception at Britannia hotel

Welcome drinks and snacks will be served from 19 to 22 in Britannia hotel. The female student choir CANDISS will appear, and sing for us. The reception is sponsored by Nordic Semiconductor and Elektronikk.

Wednesday 25th	Social event

The social event starts by boarding busses at the conference venue. This social event is sponsored by ARM Limited.

Program:

15.45 -17.45	City tour

Guided bus tour in Trondheim. The city is 1014 years old. Cruising through the Old Town, the Old bridge, Kristiansten Fortress, stopping at vista points. Small refreshment.

18.00 -18.30	The Nidaros Cathedral

Welcome greeting by the Mayor of Trondheim, followed by organ concert.

18.30 -18.45	Walk to Britannia Hotell

Short stroll (4 blocks) to Britannia hotel. Transport will be available for those who do not want to walk to the hotel.

19.00 -22.00	Banquet at Britannia Hotell

Banquet dinner in the Palm Garden of Britannia hotel. Entertainment by local folk dance group.

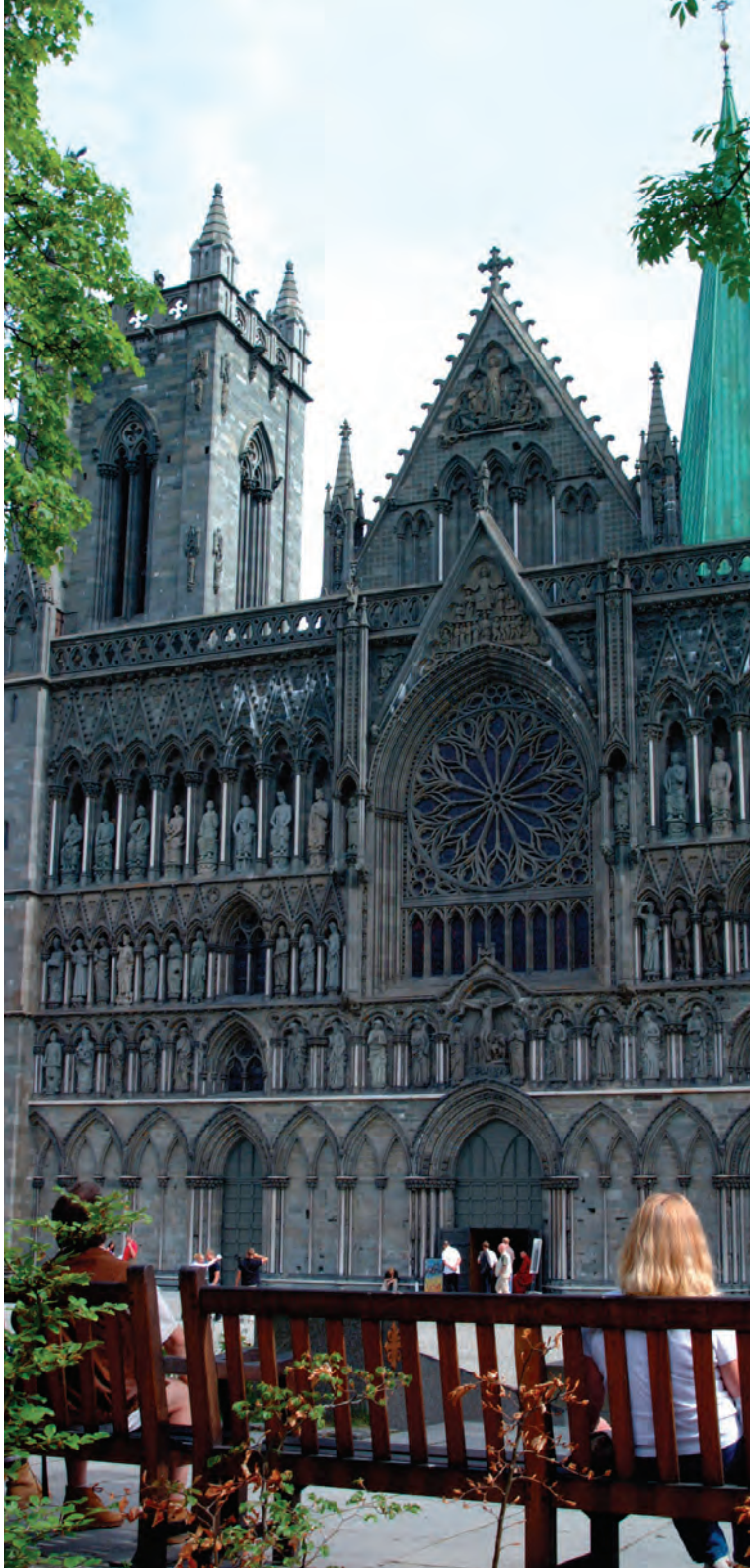
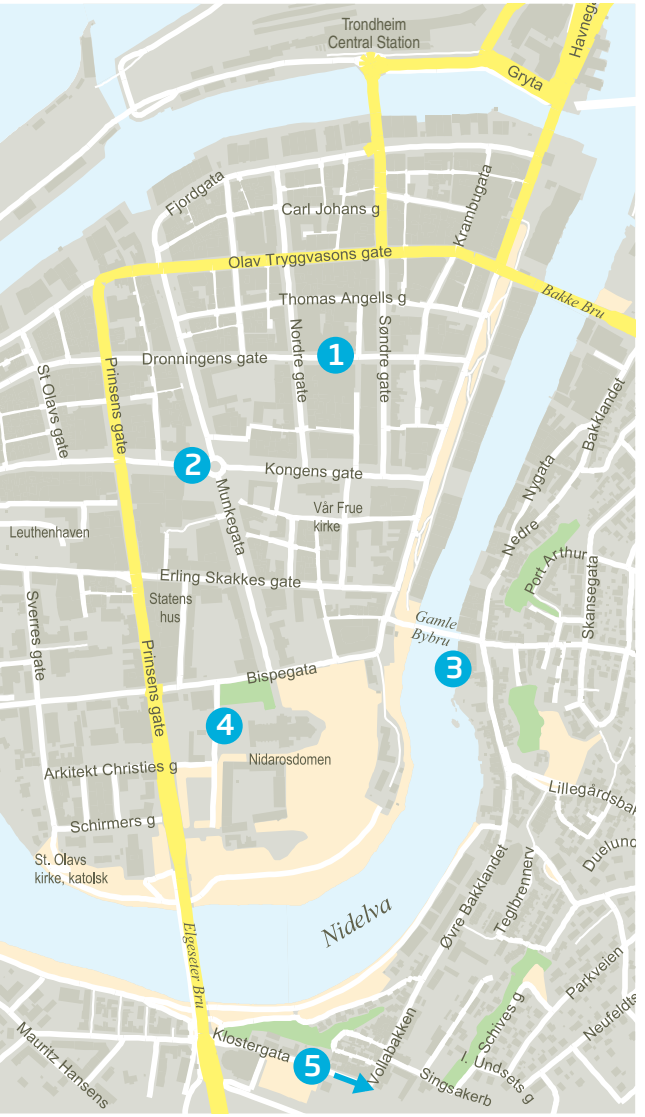


Photo: Jørn Adde © Trondheim kommune.

Map of the city

1 BRITANNIA HOTEL
2 THE CITY SQUARE
3 THE OLD BRIDGE
4 THE NIDAROS CATHEDRAL
5 REALFAGBYGGET



Plan of the venue

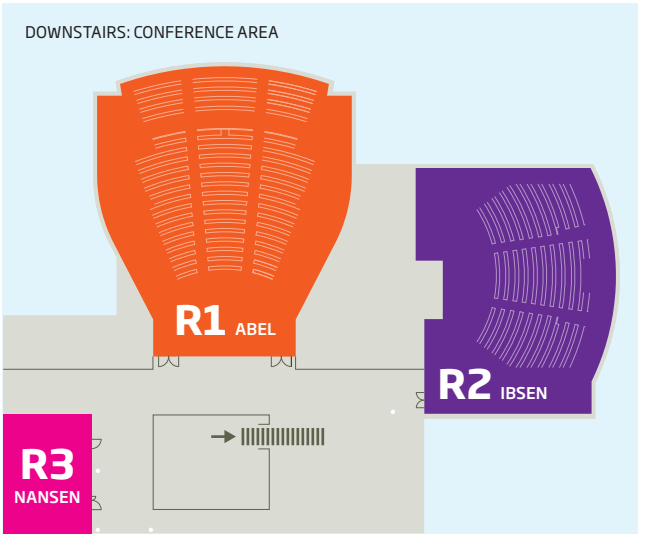
We have named the rooms in honor of some known Norwegians:

ABEL: *the mathematician Niels Henrik Abel showed there is no general algebraic solution for the roots of a any general polynomial equation of degree greater than four.*

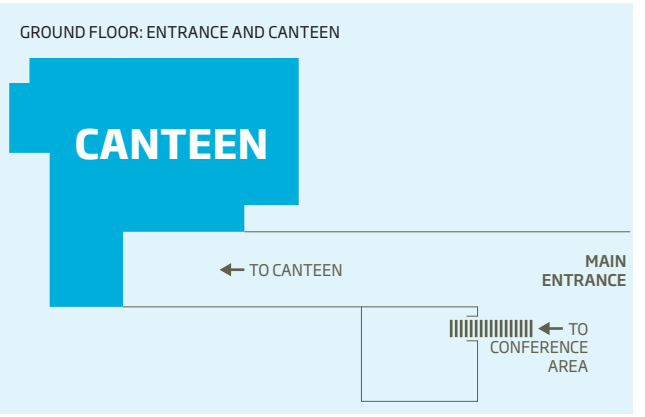
IBSEN: *the author Henrik Ibsen, known for several theatrical plays, e.g. A Doll's House.*

NANSEN: *Fridtjof Nansen, explorer, scientist, diplomat, humanitarian and Nobel laureate. He led the first crossing of the Greenland interior.*

GRIEG: *composer Edvard Grieg, best known for his Piano Concerto in A minor.*



Registration takes place outside R1 Abel. Tuesday May 24th three sessions will take place in R54 Grieg (on the 2nd floor of the 'A' building).



Monday May 23rd

→ REALFAGBYGGET

14:00 - 18:00 ETS TSS Tutorials

Tutorial A

R1 ABEL

Embedded Memory Testing: Fault Models, Test Algorithms, MBIST and Industrial Results

Said Hamdioui, Delft University, The Netherlands

Abstract: Embedded memories have become the fastest growing segment of Systems on Chip (SoC) in recent years. According to the International Technology Roadmap for Semiconductors, embedded memories will continue to dominate the increasing SoC chip area in the future, approaching 94% within one decade. Hence, these memories will severely impact all aspects of SoC manufacturing including yield, quality and reliability. Additionally, nanotechnology is causing higher levels of device-parameter variations and new failure mechanisms that are not yet well understood. Precise fault modeling to design efficient tests is therefore essential in order to keep the test cost and test time within economically acceptable limits, while keeping higher product quality.

The objective of this tutorial is to provide an overview of fault modeling and test design for memory devices. Traditional fault modeling and recent development in fault models for current and future technologies are covered. Systematic methods for designing and optimizing test patterns are presented, and supported by industrial results. Memory Built-In-Self Test, as a common industrial method to implement the test algorithms, is discussed. Last, future challenges in embedded memory testing (e.g., in fault modeling, test design) are highlighted.

Tutorial B

R9 ONSAGER

Design for Test and Fault Tolerance for Nanoscale Circuits

Sybille Hellebrand, Universität Paderborn, Germany

Abstract: Nanoscale integration comes along with an increased variability of circuit parameters, as well as with growing soft error rates. To achieve acceptable yield and to ensure a reliable system operation in the field, a "robust" design must compensate both permanent and transient faults to a certain extent. Testing becomes particularly difficult in this context, because different instances of a circuit may need different test sets, and a robust design style makes it hard to distinguish between critical and non-critical failures during test. Moreover, a pass/fail-test is no longer sufficient, but the remaining robustness for system operation must be determined ("quality binning").

This tutorial shows how classical fault tolerant architectures can be used for yield and reliability improvement, and also introduces emerging self-calibrating and adaptive architectures. Furthermore, the challenges of testing robust systems are discussed, and specific DfT solutions are presented. Finally, techniques for analyzing the robustness properties of a circuit are explained.

19:00-22:00 Reception at Britannia Hotel

Registration from 18:30. Snacks and refreshments are served.
Entertainment: Student choir CANDISS.

Tuesday May 24th

09:00-11:00 Opening

R1 ABEL

Moderator: *Ondřej Novák , TU Liberec, Czech Republic, ETS'10 General Chair*

Welcome Address
Einar J. Aas, Norwegian University of Science and Technology, Norway – ETS'11 General Chair

Technical Program Overview
Erik Larsson, Linköping University, Sweden – ETS'11 Program Chair

Presentation of ETS'10 Best Paper Award
Sybille Hellebrand, Universität Paderborn, Germany – ETS'10 Program Chair

TTTC Award Ceremony
Yervant Zorian, Synopsys Inc., USA

09:30-10:15 Keynote

The Truths and Myths of Embedded Computing

Shekhar Borkar, Intel Corporation, USA

Abstract: Computers have become ubiquitous, from powerful data centers housing supercomputing clusters to tiny microcontrollers in your toothbrush. However, embedded computing discipline does not get its fair share of attention. In this talk we will define the scope of embedded computing, compare it to general purpose computing with appropriate metrics, challenge the myths that float around and uncover the truths. We will discuss challenges in architecture, design, and test of future embedded computers, which will become even more ubiquitous by becoming part of the general purpose computers.

Bio: Shekhar Borkar graduated with M.Sc in Physics from University of Bombay in 1979, MSEE from University of Notre Dame in 1981 and joined Intel Corp, where he worked on the 8051 family of microcontrollers, and Intel's supercomputers. His research interests are low power, high performance digital circuits, and high speed signaling. Shekhar is an Intel Fellow, an IEEE Fellow, and Director of Exascale Technologies in Intel Labs.

10:15 - 11:00 Keynote

From custom design to high volume design and manufacture - shift in major validation and test challenges

Frank Berntsen, Nordic Semiconductor, Norway

Abstract: The talk will start with a historical view on the challenges of test and verification as seen from a company that has evolved from design house for moderate volume ASIC to a fabless semiconductor company for high volume consumer wireless products. The challenges have changed over 15 technology nodes and changing market focus in addition to the volume increase. Another part of the talk will address the challenges today as seen from a company that shall deliver world class SoC with analog and RF in high volume where the complexity of the products is not in very high gate counts or leading edge nm technology nodes.

Bio: Frank Berntsen received his M. Sc. in Computer Aided Design from Norwegian University of Science and Technology (NTNU) in 1980. During 1980 - 1983, he was Research engineer with Sintef, Trondheim working with IC design and CAD tool programming. In 1983, he co-founded Nordic VLSI (now Nordic Semiconductor). During 1983 - 1995 he was with Nordic Semiconductor, to which he returned in 1997 after two years at Alcatel Micro Electronics, where he had a position in IC design and project management. At Nordic Semiconductor he has held many positions, and is currently Chief Scientist. He has been central in defining the companies design and production strategies and methodologies, including design for test and ATE test solutions.

Program at a glance

Monday May23rd

14:00 - 18:00	**AUDITORIUM R1** **(TSS@ETS) Track A** Embedded Memory Testing: Fault Models, Test Algorithms, MBIST and Industrial Results	**AUDITORIUM R9** **(TSS@ETS) Track B** Design for Test and Fault Tolerance for Nanoscale Circuits

Tuesday May24th

	R1 ABEL	R2 IBSEN	R3 NANSEN	R54 GRIEG	LOBBY AREA/CANTEEN
09:00	Opening session				
11:00					Posters and coffee
12:00	Converter testing	Security	Industrial Testing (Vendor session)	Power switches	
13:00					Lunch in canteen
14:30	Emerging technologies	3D technology	Mixed signal and RF test		
16:00					Posters and coffee
17:00	Dependability	Test data compression, compaction and diagnosis	Test Equipment 1 (Vendor session)		
18:30			PhD forum		

Wednesday May25th

	R1 ABEL	R2 IBSEN	R3 NANSEN	LOBBY AREA/CANTEEN
09:00	Advances in Test	Contactless and memory testing	Test-EDA (Vendor session)	
10:30				Posters and coffee
11:30	ATPG 1	Analog production test	Test Equipment 2 (Vendor session)	
13:00				Lunch in canteen
14:30	**Embedded tutorial A:** Formal Verification of SoC – Industrial Experiences and Scientific Perspective		**Embedded tutorial B:** Towards Variation-Aware Test	
15:45				Social event – bus departure

Thursday May26th

	R1 ABEL	R2 IBSEN	R3 NANSEN	LOBBY AREA/CANTEEN
09:00	ATPG 2	Post silicon debug	Industrial testing (Vendor session)	
10:30				Poster Session 4 and coffee. TTTC's E. J. McCluskey Best Doctoral Thesis Award and Student Work-in-Progress
11:30	**Panel A** Working Silicon versus Working Board/System: Closing the Gap	**Panel B** Taking the Sense and Nonsense Out of Temperature-Aware Testing	**Panel C** BIST for non-digital IPs: can we (do we need to) estimate test costs before production?	
13:00				Lunch in canteen
14:30	Session 7 – Diagnosis			
16:00	Closing			

Fringe workshops: DDT, IWPVTD, LPonTR. See links to each workshop on the ETS'11 Web site.
Starts Thursday May 26 at 16:45. Continues Friday May 27 at 08:30 and finishes at 16:00.

11:00-12:00 Coffee and Posters (poster session 1)

Online Univariate Outlier Detection in Final Test: A Robust Rolling Horizon Approach

Harm Bossers, Johann Hurink, Gerard Smit (University of Twente - The Netherlands)

Timing Vulnerability Factors of Ultra Deep-Sub-Micron CMOS

Massoud Mokhtarpourghahahroodi, Mark Zwolinski (University of Southampton - United Kingdom)

F-Scan Test Generation Model for Delay Fault Testing at RTL using Standard Full Scan ATPG

Satoshi Ohtake, Hideo Fujiwara (Nara Institute of Science and Technology - Japan)

Viterbi-based Efficient Test Data Compression

Dongsoo Lee, Kaushik Roy (Purdue University - USA)

Memory Test Optimization for Parasitic Bit Line Coupling in SRAMs

Sandra Irobi, Zaid Al-Ars, Said Hamdioui (Delft University of Technology - Netherlands)

A Novel SRAM-Cell based Input Vector Monitoring Concurrent BIST architecture

Ioannis Voyiatzis, Costas Efstathiou, Hera Antonpoulou (TEI of Patras - Greece)

12:00-13:00 Session 1

R54 GRIEG Power switches

Moderators: *Bram Kruseman, NXP Semiconductors, The Netherlands*
Arnaud Virazel, LIRMM, France

Improved DFT for Testing Power Switches

S. Saqib Khursheed, Xiaoyu Huang, Sheng Yang, Bashir Al-Hashimi (University of Southampton - United Kingdom), David Flynn (ARM Limited - United Kingdom) (Scientific)

Signature Analysis for Testing, Diagnosis, and Repair of Multi-Mode Power Switches

Zhaobo Zhang (Duke University - USA), Xrysovalantis Kavousianos (University of Ioannina - Greece), Yan Luo (Duke University - USA), Yiorgos Tsiatouhas (University of Ioannina - Greece), Krishnendu Chakrabarty (Duke University - USA) (Scientific)

R2 IBSEN Security

Moderators: *Said Hamdioui, Delft University of Technology, The Netherlands*
Virendra Singh, Indian Institute of Science, India

Scan attacks and countermeasures in presence of scan response compactor

Jean Darolt, Giorgio Di Natale, Marie-Lise Flottes, Bruno Rouzeyre (LIRMM - France) (Scientific)

Challenge-response based secure test wrapper for testing cryptographic circuits

Amitabh Das, Miroslav Knezevic, Stefaan Seys, Ingrid Verbauwhede (Katholieke Universiteit Leuven - Belgium) (workshop)

R1 ABEL Converter testing

Moderators: *Hans Kerkhoff, Twente University, The Netherlands*
Haralampos Stratigopoulos, TIMA, France

Memory Optimized Two Stimuli INL Test Method for ADCs and DAC-ADC pairs

Esa Korhonen, Juha Kostamovaara (University of Oulu - Finland) (Scientific)

Signature Based Dynamic Test for High Precision Sigma-Delta ADCs

Sehun Kook, Abhijit Chatterjee (Georgia Institute of Technology - USA) (Scientific)

R3 NANSEN Industrial Testing (Vendor session)

Moderators: *Xinli Gu, Huawei, USA*
Kim Petersén, Ericsson, Sweden

Verification of Graphical Processing Units in ARM

Øystein Gjermundnes (ARM – Norway)

On Evaluation of Delay Fault BIST in Low-Power CMOS Device

Tor Erik Leistad, Frode Pedersen (Atmel – Norway), Einar J. Aas (Norwegian University of Science and Technology)

13:00-14:30 Lunch

14:30-16:00 Session 2

R2 IBSEN 3D technology

Moderators: *Nicola Nicolici, McMaster University, Canada*
Urban Ingelsson, Linköping University, Sweden

A Pre- and Post-Bond Self-Testing and Calibration Methodology for SAR ADC Array in 3-D CMOS

Imager Xuan-Lun Huang, Ping-Ying Kang, Jiun Lang Huang (National Taiwan University - Taiwan), Yung-Fa Chou, Yung-Pin Lee, Ding-Ming Kwai (Industrial Technology Research Institute - Taiwan) (Scientific)

Layer Redundancy Based Yield Improvement for 3D Wafer-to-Wafer Stacked Memories

Mottaqiallah Taouil, Said Hamdioui (Delft University of Technology - The Netherlands) (Scientific)

DfT Architecture for 3D-SICs Having Multiple Towers

Chun-Chuan Chi (National Tsing Hua University - Taiwan), Erik Jan Marinissen (IMEC - Belgium), Sandeep Kumar Goel (TSMC - USA), Cheng-Wen Wu (National Tsing Hua University - Taiwan) (Scientific)

R1 ABEL Emerging technologies

Moderators: *Krishnendu Chakrabarty, Duke University, USA*
Michel Renovell, LIRMM, France

Power Aware Post-Manufacture Tuning of Analog Nanocircuits

Aritra Banerjee, Azad Naeemi, Abhijit Chatterjee (Georgia Institute of Technology - USA) (Scientific)

Tomographic Testing and Validation of Probabilistic Circuits

Alexandru Paler (University of Passau - Germany), Armin Alaghi (University of Michigan - USA), Ilia Polian (University of Passau - Germany), John Hayes (University of Michigan - USA) (Scientific)

Fault Masking and Diagnosis in Reversible Circuits

Masoud Zamani, Navid Farazmand (Northeastern University - USA), Mehdi Tahoori (Karlsruhe Institute of Technology - Germany) (Scientific)

R3 NANSEN Mixed-signal and RF test

Moderators: *Salvador Mir, TIMA, France*
Jerzy Dabrowski, Linköping University, Sweden

Extraction of EVM from Transmitter System Parameters

Afsaneh Nassery, Sule Ozev (Arizona State University - USA), Marian Verhelst (Intel Corp. - USA, Mustapha Slamani (IBM - USA) (Scientific)

A mixed-signal test bus and analog BIST with 'unlimited' time and voltage resolution

Stephen Sunter (Mentor Graphics - Canada), Aubin Roy (LogicVision, Inc. - Canada) (Scientific)

Tree-Based Classification for Predicting Analogue Device Test Failures

Shaji Krishnan (TNO - The Netherlands), Hans Kerkhoff (University of Twente - The Netherlands) (Workshop)

16:00-17:00 Poster session 2

FPGA soft error recovery mechanism with small hardware overhead

Uros Legat, Anton Biasizzo, Franc Novak (Jozef Stefan Institute - Slovenia)

I-BIRAS: Interconnect Built-In Self-Repair and Adaptive Serial-ization for Inter-Die Communication in 3D Integrated Systems

Michael Nicolaidis, Vladimir Pasca, Lorena Anghel (TIMA Laboratory - France)

A Hardware-Based Approach for Fault Detection in RTOS-Based Embedded Systems

Dhiego Silva, Kleber Stangherlin, Leticia Maria Veiras Bolzani, Fabian Vargas (Pontifícia Universidade Católica do Rio Grande do Sul - Brazil)

High-Performance Diagnostic Fault Simulation on GPUs

Min Li, Michael Hsiao (Virginia Tech - USA)

Dynamic Test Set Selection using Implication-Based On-Chip Diagnosis

Nuno Alves, Yiwen Shi (Brown University - USA), Jennifer Dworak (Southern Methodist University - USA), Kundan Nepal (Bucknell University - USA), Iris Bahar (Brown University - USA)

A Low-cost Emulation System for fast Co-verification and Debug

Michelangelo Grosso, Jorge Lagos-Benites, Luca Sterpone, Matteo Sonza Reorda (Politecnico di Torino - Italy), Giorgio Audisio, Mauro Pipponzi, Marco Sabatini (Pirelli Tyre - Italy)

17:00-18:30 Session 3

R1 ABEL Dependability

Moderators: *Massimo Violante, Politecnico di Torino, Italy*
Lorena Anghel, TIMA, France

AVF Analysis Acceleration through Hierarchical SFI

Michail Maniatakos (Yale University - USA), Chandrasekharan Tirumurti, Abhijit Jas (Intel Corporation - USA), Yiorgos Makris (Yale University - USA) (Scientific)

Using Design-for-Test Features to implement Functional Safety for Automotive Microcontrollers

Heiko Ahrens (Freescale Inc. - Germany), Marco Casarsa (STMicroelectronics - Italy), Thomas Koch, Claudia Latzel, Bernd Rehberger (Freescale Inc. - Germany), Helmut Lang (Freescale Semiconductor - Germany) (Workshop)

Efficient Fault Detection Architecture Design of Latch-based Low Power DSP/MCU Processor

Hai Yu, Michael Nicolaidis, Lorena Anghel, Nacer-Eddine Zergainoh (TIMA Laboratory - France) (Scientific)

R2 IBSEN Test data compression, compaction and diagnosis

Moderators: *Xrysovalantis Kavousianos, University of Ioannina, Greece*
Nur Touba, University of Texas at Austin, USA

Reduced ATE Interface for High Test Data Compression

Jerzy Tyszer (Poznan University of Technology - Poland), Janusz Rajski, Grzegorz Mrugalski, Nilanjan Mukherjee, Dariusz Czysz (Mentor Graphics - USA) (Scientific)

Toggle-Based Masking Scheme for Clustered Unknown Response Bits;

Ozgur Sinanoglu (New York University - Abu Dhabi - United Arab Emirates) (Scientific)

Structural In-Field Diagnosis for Random Logic Circuits

Alejandro Cook, Hans-Joachim Wunderlich (Universität Stuttgart - Germany), Ulrich Abelein (AUDI AG -Germany), Melanie Elm (Universität Stuttgart - Germany) (Scientific)

NANSEN Test Equipment 1 (Vendor session)

Moderators: *Gunnar Carlsson, Ericsson, Sweden*
Paolo Bernardi, Politecnico di Torino, Italy

Wafer-Level RF MEMS Devices Characterization in Cryogenic Environment

Andrej Rumiantsev, Frank-Michael Werner, Stojan Kanev - Cascade Microtech

Innovative techniques for efficient Non Deterministic Protocol testing on ATE

Oscar Solano Jimenez and Andre Wegener - Verigy, USA

Automated Test Program Generation for Automotive Devices

Peter Huber, Jon Vollmar - Teradyne; Anke Drappa, Robert Bosch GmbH, Germany

18:30-20:00 PhD forum

NANSEN

Moderator: *Ilia Polian, Universität Passau, Germany*

Christian Berger, Automotive Safety Technologies GmbH, Germany

Automating Acceptance Tests for Sensor- and Actuator-based Systems on the Example of Autonomous Vehicles

Urban Ingelsson, Linköpings universitet, Sweden

Investigation into Voltage and Process Variation-Aware Manufacturing Test

Viacheslav Izosimov, EIS By Semcon, Sweden

Scheduling and Optimization of Fault-Tolerant Distributed Embedded Systems

Esa Korhonen, University of Oulu, Finland

On-chip Testing of A/D and D/A Converters. Static Linearity Testing without Statistically Known Stimulus

Alberto Scionti, Politecnico di Torino, Italy

Defect oriented memory test and repair at the nanometer design scale

Wednesday May 25th

09:00-10:30 Session 4

R1 ABEL Advances in test

Moderators: *Tomoo Inoue, Hiroshima City University, Japan*
Gert Jervan, Tallinn Technical University, Estonia

Accelerating RTL Fault Simulation through RTL-to-TLM Abstraction

Nicola Bombieri, Valerio Guarnieri, Franco Fummi (University of Verona - Italy) (Scientific)

Improving Reliability in NoCs by Application-Specific Mapping Combined with Adaptive Fault-Tolerant Method in the Links

Anelise Kologeski, Caroline Concatto, Luigi Carro, Fernanda Kastensmidt (Universidade Federal do Rio Grande do Sul - Brazil) (Scientific)

Latency Analysis for Sequential Circuits

Alexander Finder, André Sülflow, Goerschwin Fey (University of Bremen - Germany) (Scientific)

R2 IBSEN Contactless and memory testing

Moderators: *Zaid Al-Ars, Delft University of Technology, The Netherlands*
Hans Manhaeve, Q-Star Test nv, Belgium

Effectiveness of Memory Test Algorithms and Analysis of Fault Distribution in SRAMs

Michael Linder, Alfred Eder (University of Applied Sciences Augsburg - Germany), Klaus Oberlaender, Martin Huch (Infineon Technologies AG- Germany) (Workshop)

Variability Analysis of an SRAM Test Chip

Renan Alves Fonseca, Luigi Dilillo, Alberto Bosio, Patrick Girard, Serge Pravossoudovitch, Arnaud Virazel (LIRMM - France), Nabil Badereddine (Infineon - France) (Workshop)

Innovative I/O PAD for Direct Contact and Contactless Testing

Mauro Scandiuzzo, Luca Perilli, Salvatore Cani, Roberto Cardu, Luca Perugini, Simone Spolzino, Roberto Canegallo, Eleonora Franchi (ST Lab- Arces University of Bologna - Italy) (Scientific)

R3 NANSEN Test-EDA (Vendor session)

Moderators: *Bill Eklow, Cisco, USA*
Zdenek Kotasek, Brno University of Technology, Czech Republic

Digital test and diagnosis advances reduce risk with new fabrication technologies

Geir Eide (Mentor Graphics - USA)

Accelerating Time-to-Quality

Yervant Zorian (Synopsys Inc. - USA)

Evolution in low pin count, 3D and low power test

Michael O'Sullivan (Cadence - USA)

10:30-11:30 Coffee and Posters (poster session 3)

Revisiting Application-Dependent Test for FPGA devices

Alessandro Cilardo, Carmelo Lofiego, Nicola Mazzocca (University of Naples Federico II - Italy)

Temperature-Variation-Aware Test Pattern Optimization

Tomokazu Yoneda, Makoto Nakao, Michiko Inoue (Nara Institute of Science and Technology - Japan), Yasuo Sato (Kyusyu Institute of Technology - Japan), Hideo Fujiwara (Nara Institute of Science and Technology - Japan)

Analysis and Mitigation of Electromigration in RF Circuits: An LNA Case Study

Ramachandran Venkatasubramanian, Doohwang Chang, Sule Ozev (Arizona State University - USA)

Enhancement of Clock Delay Faults Testing

Yoshinobu Higami, Hiroshi Takahashi, Shin-ya Kobayashi (Ehime University - Japan), Kewal Saluja (Univ. of Wisconsin - Madison - USA)

Dual Edge Triggered Flip-Flop for Noise Aware Design

Yukiya Miura (Tokyo Metropolitan Univ. - Japan)

On High-Quality Test Pattern Selection and Manipulation

Feng Yuan, Xiao Liu, Qiang Xu (The Chinese University of Hong Kong - Hong Kong)

11:30-13:00 Session 5

R1 ABEL ATPG 1

Moderators: *Saqib Khursheed, University of Southampton, UK*
Stephan Eggersglüß, Universität Bremen, Germany

An Approach for Quantifying Path Correlation in Digital Circuits without any Path or Segment Enumeration

Stelios Neophytou (University of Nicosia - Cyprus), Kyriakos Christou, Maria Michael (University of Cyprus - Cyprus) (Scientific)

Constraint-Based Hierarchical Untestability Identification for Synchronous Sequential Circuits

Jaan Raik, Anna Rannaste, Maksim Jenihhin, Taavi Viilukas (Tallinn University of Technology - Estonia), Hideo Fujiwara (Nara Institute of Science and Technology - Japan), Raimund Ubar (Tallinn Technical University - Estonia) (Scientific)

A Functional Power Evaluation Flow for Defining Test Power Limits during At-Speed Delay Testing

Miroslav Valka, Alberto Bosio, Luigi Dilillo, Patrick Girard, Serge Pravossoudovitch, Arnaud Virazel (LIRMM - France), Ernesto Sanchez, Mauricio De Carvalho, Matteo Sonza Reorda (Politecnico di Torino - Italy) (Scientific)

R2 IBSEN Analog production test

Moderators: *Jochen Rivoir, Verigy, Germany*
Florence Azais, LIRMM, France

A Robust Metric for Screening Outliers from Analogue Product Manufacturing Tests Responses

Shaji Krishnan (TNO - The Netherlands),
Hans Kerkhoff (University of Twente - The Netherlands) (Scientific)

Fast and Accurate DPPM Computation for Analog/RF Circuit Using Model Based Filtering

Ender Yilmaz (Arizona State University - USA),
Sule Ozev (Arizona State University - USA) (Scientific)

Finding Resilience Weak Spots in Mixed-Signal Circuits for Automotive Applications

Vincent Kerzerho, Hans Kerkhoff (University of Twente - The Netherlands),
Gert-Jan Bollen (NXP Semiconductors - The Netherlands),
Yizi Xing (NXP Semiconductors - The Netherlands) (Workshop)

R3 NANSEN Test equipment 2 (Vendor session)

Moderators: *Jennifer Dworak, Southern Methodist University, USA*
Manoj S Gaur, Malaviya National Institute of Technology, India

Cost Effective Testing in the New Era

Peter Cockburn (LTX-Credence - USA)

Advances in Software Defined Instrumentation for Semiconductor Test

Stein Arild Nordrum (National Instruments - Norway)
Erik Hilten (National Instruments - The Netherlands)

Supplementing Structural Test Approaches with In-System Diagnostics for Improved Coverage

Clint Ostrander (Kozio -USA)

13:00-14:30 Lunch

14:30-15:30 Embedded tutorials

Embedded tutorial A

R1 ABEL

Moderator: *Matteo Sonza Reorda, Politechnico di Torino, Italy*

Formal Verification of Systems-on-Chip - Industrial Experiences and Scientific Perspectives

Wolfgang Kunz (Technische Universität Kaiserslautern - Germany)

Abstract: Even after years of progress in the field of formal property checking many designers in industry still consider simulation as their most powerful and versatile instrument when verifying complex SoCs. Often, formal techniques are only conceded a minor role. At best, they are viewed as nice-to-have additions to conventional simulation, for example as a tool for "hunting bugs" in corner cases. On the other hand, in some parts of industry, a paradigm shift can be observed. Verification methodologies have emerged that involve property checking comprehensively, and in a systematic way.

In this embedded tutorial, we review the scientific foundations of modern formal verification tools. Basic algorithmic concepts of formal verification tools are related to notions of automatic test generation. The main focus of this tutorial, however, will be to demonstrate how basic algorithmic issues and the choice of computational models influence industrial verification methodologies. We report on experiences from large-scale industry projects. A systematic property checking methodology is presented as it has evolved in some parts of the industry. Furthermore, we attempt to identify the bottlenecks of today's technology and to outline specific scientific challenges.

While formal property checking for individual SoC modules can be considered fairly mature it is well-known that there are tremendous obstacles when moving the focus from modules to the entire system. On the system level, today's verification tools run into severe capacity problems. These do not only result from the sheer size of the system but also from the different nature of the verification tasks. In this tutorial, we will analyze and discuss these challenges, relating to well-known abstraction approaches. A scenario will be presented how formal architectural models can be created that pave the way to a new SoC design methodology which integrates formal verification in a more natural way, thus significantly reducing its costs.

Embedded tutorial B

R3 NANSEN

Moderator: *Pete Harrod, ARM Limited, UK*

Towards Variation-Aware Test Methods

Ilia Polian (University of Passau - Germany), Bernd Becker (University of Freiburg - Germany), Sybille Hellebrand (University of Paderborn - Germany), Hans-Joachim Wunderlich (Universität Stuttgart - Germany), Peter Maxwell (Aptina Imaging - USA)

Abstract: Nanoelectronic circuits are increasingly affected by massive statistical process variations, leading to a paradigm shift in both design and test area. In circuit and system design, a broad class of methods for robustness like statistical design and self calibration has emerged and is increasingly used by the industry. The test community's answer to the massive-variation challenge is currently adaptive test. The test stimuli are modified on the fly (during test application) based on the circuit responses observed. The collected circuit outputs undergo statistical post-processing to facilitate pass/fail classification. We will present fundamentals of adaptive and robust test techniques and their theoretical background. While adaptive test is effective, the understanding how it covers defects under different process parameter combinations is not fully established yet with respect to algorithmic foundations. For this reason, novel analytic and algorithmic approaches in the field of variation-aware testing will also be presented in the tutorial. Coverage of defects in the process parameter space is modeled and maximized by an interplay between special fault simulation and multi-constrained ATPG algorithms. These systematic approaches can complement adaptive test application schemes to form a closed-loop system that combines analytical data with measurement results for maximal test quality.

15:45-22:00 Social event

Starting with guided bus tour of the 1014 years old city, organ concert in the Nidaros Cathedral, continue with banquet in Britannia Hotel.

Thursday May 26th

09:00-10:30 Session 6

R2 IBSEN Post-silicon debug

Moderators: *Frank Poehl, Intel Mobile Communications, Germany*
Mehdi B. Tahoori, Karslruhe Institute of Technology, Germany

Optimization of Assertion Placement in Time-Constrained Embedded Systems

Giuseppe di Guglielmo (University of Verona - Italy), Zebo Peng (Linköping University - Sweden), Masahiro Fujita (Univ. of Tokyo - Japan), Franco Fummi (University of Verona - Italy), Viacheslav Izosimov (EIS By Semcon - Sweden), Graziano Pravadelli, Michele Lora (University of Verona - Italy) (Scientific)

On Post-silicon Root-Cause Analysis and Debug Using Enhanced Hierarchical Triggers

M. H. Neishaburi, Zeljko Zilic (McGill University - Canada) (Workshop)

Post-Silicon Functional Failing-Test Generation through Evolutionary Computation

Ernesto Sanchez, Giovanni Squillero, Alberto Tonda (Politecnico di Torino - Italy) (Workshop)

R1 ABEL ATPG 2

Moderators: *Jaan Raik, Tallinn, Technical University, Estonia*
Mahmut Yilmaz, AMD, USA

On Timing-Aware ATPG using Pseudo-Boolean Optimization

Stephan Eggersglüß, Rolf Drechsler (University of Bremen - Germany) (Workshop)

Critical Fault-Based Pattern Generation for Screening SDDs

Fang Bao, Ke Peng (University of Connecticut - USA), Mahmut Yilmaz, Krishnendu Chakrabarty (Duke University - USA), LeRoy Winemberg (FreeScale Semiconductor - USA), Mohammad Tehranipoor (University of Connecticut - USA) (Scientific)

Test pattern generation for Multi-cycle Power Droop using SAT solver

Susmita Sur-Kolay (Indian Statistical Institute - India), Santanu Bhowmick (NVidia Corporation - India), Onkar Tiwari (Nvidia Graphics Pvt Ltd - India), Bhargab Bhattacharya, Debasis Mitra (Indian Statistical Institute - India) (Workshop)

R3 NANSEN Industrial testing (Vendor session)

Moderators: *Giorgio di Natale, LIRMM, France*
Michael Hsiao, Virginia Tech., USA

Boundary-scan (IEEE 1149.1) 20 years

Cor Stork (JTAG Technologies - The Netherlands)

JTAG / Boundary Scan and JTAG Emulation for board level test and programming and design verification

Jan Heiber (Goepel Electronics - Germany)

FPGA-Enabled Embedded Instrumentation Platform

Artur Jutman (Tallinn University of Technology - Estonia), Igor Aleksejev (Testonica - Estonia), Sergej Devadze (Tallinn University of Technology - Estonia)

10:30-11:30 Coffee and Posters (poster session 4) - R1 (Abel)

TTTC's E. J. McCluskey Best Doctoral Thesis Award, and Student Work-in-Progress;

Christian Berger, Automotive Safety Technologies GmbH, Germany

Automating Acceptance Tests for Sensor- and Actuator-based Systems on the Example of Autonomous Vehicles

Urban Ingelsson, Linköpings Universitet, Sweden

Investigation into Voltage and Process Variation-Aware Manufacturing Test

Viacheslav Izosimov, EIS By Semcon, Sweden

Scheduling and Optimization of Fault-Tolerant Distributed Embedded Systems

Esa Korhonen, University of Oulu, Finland

On-chip Testing of A/D and D/A Converters. Static Linearity Testing without Statistically Known Stimulus

Alberto Scionti, Politecnico di Torino, Italy

Defect oriented memory test and repair at the nanometer design scale

+ student work-in-progress posters

11:30-13:00 Panels

Panel A

R1 ABEL

Working Silicon versus Working Board/System: Closing the Gap

Abstract: "Working" silicon at device level does not mean the device will work in a system environment, where multiple devices are connected via boards, backplane connectors and chassis, and software is installed in the hardware to control system operation. Root-causing any malfunction in such a complicated environment has proven to be extremely difficult; however it is critical to pinpoint these issues and fix any silicon production-related process problems, and therefore achieve cost savings. The panel will discuss and debate solutions that are needed to bridge the gap between "working silicon" and "working board/system".

Organizer: *Krishnendu Chakrabarty, Duke University, USA*
Moderator: *Xinli Gu, Huawei Technologies, USA*

Panelists: *Bill Eklow, Cisco Systems, USA*
Artur Jutman, Tallinn Technical University, Estonia
Cuiqin Li, Huawei Technologies, USA
Gunnar Carlsson, Ericsson, Sweden
Teresa McLaurin, ARM, UK
Jun Qian, AMD, China

Panel B

R2 IBSEN

Taking the Sense and Nonsense Out of Temperature-Aware Testing

Abstract: Test engineers are used to find their sweet spot in the trade-off between Good (sufficient test quality), Cheap (in terms of extra silicon area and test execution costs), and Fast (test development time). This sweet spot is on the move, due to the inclusion of power dissipation and, more recently, temperature in the trade-off equation. Temperature-aware testing is at least a two-edged sword. Chips need to be tested varying temperature conditions, to expose specific defects and to mimic operational conditions. On the other hand, switching activity during test is typically higher than during normal operation, and we should take care not to overheat the DUT and get false test results. The experts on this panel take a detailed look at the sense (and nonsense) of temperature-aware testing, including defects, on-chip sensors, the infrastructure to control and read those sensors, external equipment heating, computing vs. automotive vs. mobile conditions, the impact of 3D stacking, cooling, etc.

Organizers: *Bernd Becker - Freiburg University, Germany*
Erik Jan Marinissen - IMEC, Belgium
Moderator: *Bashir Al-Hashimi - Southampton University, UK*

Panelists: *Rob Aitken - ARM, USA*
Edmund Cheng - Gradient Design Automation, USA
Holger Engelhard - Verigy, Germany
Bram Kruseman - NXP Semiconductors, The Netherlands
Zebo Peng - Linköping University, Sweden

Panel C

R3 NANSEN

Built-in test for non-digital IPs: can we (do we need to) estimate test costs before production?

Abstract: Numerous built-in test techniques for mixed-signal/RF have been made available in the past. Nevertheless, very few have made it to actual products. Reasons for this appear to be varied, including direct costs, indirect costs (or test quality), lack of flexibility and risk. Especially in high-volume production and when cost margins are single digit percentages, industrial

reasons for any action are almost always related to cost. On one hand, built-in test adds direct costs such as area and pin overhead, or performance degradation that are easily quantified, while significantly reducing equipment costs. On the other hand, built-in test affects indirect costs such as defect level and yield loss, which are much harder to quantify. These indirect costs represent a major source of uncertainty for adopting any new test technique, in particular built-in tests. Calculating these costs can only be done accurately at production testing, but once in production, it is no longer possible to modify the technique if it does not perform well. This panel will debate what is needed to escape this catch, eventually providing directions on what is needed for mixed-signal/RF built-in test to be adopted.

Organizer: *S. Mir (TIMA Laboratory, France)*
Moderator: *H. Kerkhoff (University of Twente, The Netherlands)*

Panelists: *Jochen Rivoir (Verigy, Germany)*
Steve Sunter (Mentor Graphics, USA)
Frank Poehl (Intel Mobile Communications, Germany)
Christophe Kelma (NXP Semiconductors, France)
Sule Ozev (Arizona State University, USA)

13:00-14:30 Lunch

R1 ABEL

14:30 - 16:00 Session 7 - Diagnosis

Moderators: *Sybille Hellebrand, Universität Paderborn, Germany*
Hans-Joachim Wunderlich, Universität Stuttgart, Germany

Structural Test for Graceful Degradation of NoC Switches

Atefe Dalirsani (Universität Stuttgart - Germany), Stefan Holst (Universität Stuttgart - Germany), Melanie Elm (Universität Stuttgart - Germany), Hans-Joachim Wunderlich (Universität Stuttgart - Germany) (Scientific)

On Transition Fault Diagnosis Using Multicycle At-Speed Broadside Tests

Irith Pomeranz (Purdue University - USA) (Scientific)

Ranking of Suspect Faulty Blocks using Dataflow Analysis and Dempster-Shafer Theory for the Diagnosis of Board-Level Functional Failures

Hongxia Fang (Duke University - USA), Zhiyuan Wang (Cisco Systems, Inc. - USA), Xinli Gu (Cisco Systems, Inc. - USA), Krishnendu Chakrabarty (Duke University - USA) (Scientific)

16:00-16:15 Closing

Moderator: *Hans-Joachim Wunderlich, Universität Stuttgart, Germany*

2011 TTTC's E.J. McCluskey Best Doctoral Thesis Award

Ilia Polian, Universität Passau, Germany

Closing remark

Einar J. Aas, Norwegian University of Science and Technology, Norway
ETS'11 General Chair

Introduction to ETS'12

Lorena Anghel, TIMA Laboratory, France
ETS'12 General Chair

May 26 - 27 Workshops

Dependability Issues in Deep-submicron Technologies

IEEE International Workshop on Processor Verification, Test and Debug (IWPVTD'11)

Workshop on Low Power Design Impact on Test and Reliability (LPonTR)

Details on workshops on web and at site.

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