

IWPVTD'11

IEEE International Workshop on Processor Verification, Test and Debug

(In conjunction with the European Test Symposium)

Trondheim, Norway, May 27, 2011

<http://www.serc.iisc.ernet.in/~viren/IWPVTD11/>

Modern computer system and systems-on-chip are built around high speed processors in order to meet consumer demand for performance and rich functionality. The increasing size and complexity of these designs, along with time-to-market pressure, has put enormous pressure on verification to ensure bug-free design. While eliminating all bugs remains an unfulfillable dream, catching more problems earlier in the design cycle is top priority. Moreover, design complexity means that some bugs may only be discovered during post-silicon debug, mandating inclusion of built-in debug features to simplify the process.

Aggressive processor design methodologies in nanometer technologies include high speed clocks, power control, environmental awareness, and complex memory interfaces. Test and verification are needed for all of these. In addition many reliability challenges, manufacturing variations, soft errors, wearout, etc. will need to be addressed by innovative new design and test methodologies if device scaling is to continue on track as per Moore's Law to 10nm and beyond. This event will bring together the processor design, verification, and test engineers together to develop a holistic approach to develop verification, test and debug solutions.

The key objective of this workshop, planned to be held in conjunction with the European Test Symposium, is to provide an informal forum for vigorous creative discussion and debate of this area. The aim is to encourage the presentation and discussion of innovative ideas that may not yet have been fully developed for presentation at reviewed conferences to address these challenges. Additionally, the workshop invites embedded talks and tutorials on cutting edge topics related to processor test, verification, debug and reliability. Representative topics include, but are not limited to:

- Processor validation
- Low power test and validation
- Emulation and prototyping
- Statistical methods
- Software-based self-test
- Performance testing
- Reliability of processor architectures
- Reliability of processor circuits
- Test generation
- Post silicon debug
- Debug and trace architectures
- ESL techniques
- Processor test
- Timing verification techniques
- Error modeling
- Verification coverage metrics
- Design for verifiability
- System validation methodology
- Design error diagnosis
- Formal verification techniques
- Formal equivalence checking
- Software verification
- Built-in self-test for processors
- Fault tolerance

Submissions

Authors are invited to submit previously unpublished technical proposals. The proposals may be extended abstracts or full papers of upto 6 pages. Each submission should include: title, full name and affiliation of all authors, a short abstract of 50 words, and 6 to 7 keywords. Also, identify a contact author and include a complete correspondence address, phone number, fax number, and e-mail address. Submit a copy of your proposal in PDF via workshop website <http://www.serc.iisc.ernet.in/~viren/IWPVTD11/>

Submissions are due no later than **March 23, 2011 (Extended)**. Authors will be notified of the disposition of their presentation by **April 18, 2011** Authors of accepted presentations must submit the final paper by **May 10, 2011** for inclusion in the Workshop Proceedings, which will be provided to the attendees.

Organizers

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