4th IEEE International Workshop on

Impact of Low-Power design on Test and Reliability
LPonTR'11

Trondheim, Norway
May 26-27, 2011

Fringe to ETS'11

http://www.staff.ncl.ac.uk/a.bystrov/LPonTR/

http://www.iet.ntnu.no/workshop/ets2011/

Chair / Co-Chair:

Alex Bystrov, *Newcastle Univ., UK*

Patrick Girard, *LIRMM, France*

Special Session Chairs:

Ilia Polian,
Univ. Freiburg, Germany

Gert Jervan,
Tallinn Univ., Estonia

Programme Committee:

Bashir Al-Hashimi,
Univ. of Southampton, UK

Karim Arabi, *Qualcomm, USA*

Swarup Bhunia,
Case Western Reserve Univ., USA

Krish Chakrabarty, *Duke Univ., USA*

Krishna Chakravadhanula,
Cadence, USA

Luigi Dilillo, *LIRMM, France*

Peter Harrod, *ARM Ltd, UK*

Mokhtar Hirech, *Synopsys, USA*

Gert Jervan, *Tallinn Univ., Estonia*

Niraj Jha, *Princeton University, USA*

Mark Kassab, *Mentor Graphics, USA*

Sandip Kundu,
Univ. Massachusetts, USA

Erik Larsson,
Linkoping Univ., Sweden

T.M. Mak, *Intel, USA*

Hans Manhaeve, *Q-Star, Belgium*

Nicola Nicolici,
McMaster Univ., Canada

Ilia Polian, *Univ. Freiburg, Germany*

Irith Pomeranz, *Purdue Univ., USA*

Srivaths Ravi, *TI, India*

Sudhakar Reddy, *Univ. of Iowa, USA*

Juan Jose Rodriguez Andina,
Univ. Vigo, Spain

Ozgur Sinanoglu,
Univ. NYUAD, Abu Dhabi

Virendra Singh,
Indian Institute of Science, India

Mohammad Tehranipoor,
Univ. Connecticut, US

J. Paulo Teixeira, *INESC-ID, Portugal*

Nur Touba,
Univ. of Texas at Austin, USA

Seongmoon Wang, *NEC, USA*

Xiaoqing Wen,
Kyushu Inst. of Technology, Japan

Hans-Joachim Wunderlich,
Univ. of Stuttgart, Germany

Qiang Xu,
The Chinese University of Hong Kong

Call for Papers

The IEEE International Workshop on *Impact of Low Power Design on Test and Reliability* (LPonTR) aims to bring together design, reliability and test engineers and researchers to discuss the impact of advanced low-power low-voltage design methodologies of nanometer silicon systems on test and reliability. Power and thermal issues, leakage, process variations, susceptibility to environmental and operation-induced interference drive the development of low-power, process-tolerant design techniques and generate a new set of test and reliability challenges, questing for an innovative set of methodologies and tools.

You are invited to participate in LPonTR'11 by presenting work that addresses current trends, challenges and solutions in the following areas (but are not limited to):

- *Energy-reliability trade-off (inc. controlled losses) and its integration with power management*
- *Power and Thermal Issues in 3D ICs*
- *Challenges of Ultra Low-power design on test and reliability*
- *Emerging failure modes*
- *Test of SoC with power and thermal management*
- *Energy, power and process variations aware design and test*
- *Test and reliability implications of leakage*
- *Low-power/voltage DfT, Dynamic BIST, Scan and ATPG*
- *Delay, statistical and parametric testing for LP circuits*
- *Signal integrity under test*
- *Test and reliability of LP redundant systems*
- *Analog, mixed-signal and asynchronous low-power design, test and DfT*
- *EDA tools to support process-tolerant LP design*

Special Sessions:

- **"Adaptive Techniques for Energy-Reliability Trade-offs"** (chaired by I. Polian) – discussion of methods which lead to significant energy savings at the expense of controlled losses in accuracy and reliability of the calculated data; implications on the design flow.
- **"Power and Thermal Issues in 3D ICs"** (chaired by G. Jervan) – impact of power consumption and heat dissipation on the performance and reliability of 3D SoC, which includes (but not limited to) power/thermal modelling and analysis, power/thermal-aware design, power integrity, heat dissipation, thermal vias, thermal/mechanical stress and cooling mechanisms.

Submissions – The authors are invited to submit **extended abstracts**. All submissions will be peer-reviewed and accepted abstracts will be published in the informal proceedings of the workshop.
Presentations – **Full oral** presentations are 15-20 min., **short oral** are 2 min. There will be space provided for **tool demonstrations** and **poster/interactive** presentations.
Journal Publications – The best contributions will be invited for publication as full papers in a Special Section on LPonTR'11 in the ASP Journal of Low Power Electronics (JOLPE).
Formats – *extended abstracts:* 2 pages, IEEE conference layout or latex8, font 10, two columns, paper A4, no page numbering, PDF file format.
Posters: up to A0-portrait. *Format for demonstrations:* please contact the Chairs.
Communication – Please e-mail your manuscripts directly to the Chairs of LPonTR.

Key Dates:

- Submission deadline (extended): ~~7th~~ **21st March, 2011**
- Notification of acceptance : 12th April, 2011
- Final manuscript (electronic format) : 10th May, 2011

Dr. Alex Bystrov
Newcastle University
School of EECE
Newcastle upon Tyne, NE1 7RU, UK
Tel.: +44 191 222 6584
Fax: +44 191 222 8180
Email: `A.Bystrov@ncl.ac.uk`

Newcastle University

Dr. Patrick Girard
LIRMM
161 rue Ada,
34392 Montpellier cedex 05, France
Tel.: +33 467 418 629
Fax.: +33 467 418 500
Email: `girard@lirmm.fr`

LIRMM

IEEE IEEE computer society tttc