



4th IEEE International Workshop on the Impact of Low Power design on Test and Reliability (LPonTR)

Gløshaugen Campus, Trondheim, Norway
May 26-27, 2011

LPonTR'11 Programme

----- Thursday, 26th May -----

16:00 – 17:00 Registration

16:45 – 17:00 Opening Remarks (A. Bystrov, P. Girard)

17:00 – 17:30 Keynote

- **Rakesh Kumar**, Univ. of Illinois, USA
Exploiting Error Resilience in Architecture and Design of Energy Efficient Processors

17:30 – 19:30 Special Session: Power And Thermal Issues In 3D

- **Gert Gervan**, Tallinn Univ., Estonia
Introduction by the Session Chair
- **Vasilis F. Pavlidis**, **G. De Micheli**, LSI-EPFL, Lausanne, Switzerland
Through-Silicon-Vias: Menace or Refuge for 3-D ICs?

----- Coffee break -----

- **Yuksel Temiz**, **Y. Leblebici**, **S. Szczukiewicz**, **N. Borhani**, **J. R. Thome**, EPFL, Switzerland; **T. Brunschweiler**, B. Michel, IBM, Switzerland
Microchannel-Based Liquid Interlayer Cooling in High-Performance 3D Stacks
- **Aida Todri**, **A. Bosio**, **L. Dilillo**, **P. Girard**, **S. Pravossoudovitch**, **A. Virazel**, LIRMM, France
Simultaneous Power and Thermal Integrity Analysis for 3D Integrated Systems

----- Friday, 27th May -----

8:30 – 9:00 Registration

9:00 – 11:35 Special Session: Adaptive techniques for energy-reliability trade-offs

- **Ilia Polian**, Univ. of Passau, Germany
Introduction by the Session Chair
- **John P. Hayes**, University of Michigan, USA
Adapting to Physical Variations in Field-Programmable Gate Arrays
- **Shidhartha Das**, ARM, UK
Razor: Eliminating Margins for Energy-efficient Computing

----- Coffee break -----

- **Viacheslav Izosimov**, Semcon AB, Sweden
Trading-off Available Resources for Fault Tolerance in Cyber-Physical Systems
- **Rob Aitken**, ARM, USA
- Panel Discussion, Chairman **Ilia Polian**, Univ. of Passau, Germany. Panelists:
 - **Rakesh Kumar**, Univ. of Illinois, USA
 - **John P. Hayes**, University of Michigan, USA
 - **Shidhartha Das**, ARM, USA
 - **Viacheslav Izosimov**, Semcon AB, Sweden
 - **Rob Aitken**, ARM, USA

11:40-- 12:30 Regular session

- **J. Rodríguez-Araújo, J. Freijedo, Lucia Costas, J.J. Rodríguez-Andina**, Univ. of Vigo, Spain
Analysis of Power Supply Noise Robustness versus Power Consumption in FPGAs
- **James Docherty, A. Bystrov and A. Yakovlev**, Newcastle Univ., UK
Using Game Theory for Managing Power and Reliability in a Circuit

12:40

----- Lunch -----

14:00-- 15:40 Regular Session

- **Irith Pomeranz**, Purdue Univ., USA
A Local Switching Activity Metric For Functional Broadside Tests
- **F. Wu, L. Dilillo, Alberto Bosio, P. Girard**, LIRMM, France; **M. Tehranipoor**, Univ. Connecticut, USA; **K. Miyase, X. Wen**, Kyushu Institute of Technology, Japan; **N. Ahmed**, Texas Instruments, USA
Mapping Test Power to Functional Power Through Smart X-Filling for LOS Scheme
- **Tsuyoshi Iwagaki**, JAIST, Japan; **K. K. Saluja**, Univ. of Wisconsin-Madison, USA
Power-Constrained Test Generation for Hold-Time Faults Using Integer Linear Programming
- **Hassan Salmani, W. Zhao, M. Tehranipoor**, Univ. Connecticut, USA; **S. Chakravarty**, LSI Logic, USA; **P. Girard**, LIRMM, France; **X. Wen**, Kyushu Institute of Technology, Japan
Layout-Aware Pattern Evaluation and Analysis for Power-Safe Application of TDF Patterns

15:45 – 16:00 Closing Remarks (A. Bystrov, P. Girard)



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