



5th IEEE International Workshop

Impact of Low-Power Design on Test and Reliability (LPonTR)

Annecy, France
May 31- June 1, 2012

LPonTR'12 Programme

Thursday, 31st May

15:30 – 16:30 Registration

16:15 – 16:30 Opening Remarks (A. Bystrov, P. Girard)

16:30 – 17:00 Keynote

- **Robin Wilson**, STMicroelectronics, Crolles, France
Manufacturable Energy Efficient IC design “Taming the Untamed World”

17:00 – 18:40 Special Session: *Power And Thermal Issues In 3D*

- **Aida Todri-Sanial**, LIRMM, France
Introduction by the Session Chair
- **Pascal Vivet, Fabien Clermidy, and Denis Dutoit**, CEA-LETI, France
Design-for-Test and Fault Tolerant Architecture for a 3D NoC TSV-based Infrastructure

----- Coffee break -----

- **Vasilis F. Pavlidis and Giovanni De Micheli**, EPFL, Switzerland
Low-Power Pre-Bond Testable 3-D Clock Distribution Networks
- **Nicolas Peltier, Pierre Lebeaut, Philippe Duchene, Sylvian Kaiser**, DOCEA Power, France
How 3D impacts thermal budget: illustration and tool for simulation

18:40 – 19:00 Test and 3D

- **Indira Rawat** (Govt. Engineering College, Ajmer, Rajasthan, India.), **M.K. Gupta** (Maulana Azad National Institute of Technology, Bhopal, India), **Virendra Singh** (Institute of Technology, Mumbai, India)
Thermal Aware Test Scheduling of 3D SoCs (research paper)

Friday, 1st June

8:30 – 9:00 Registration

9:00 – 9:30 Keynote

- **Hans Manhaeve**, Hans Manhaeve, Qstar, Belgium
Deployment and Application of Current Testing in the Context of Low Power Design

9:30 – 11:30 Special Session: *Cross-Layer Reliability and Low Power*

- **Ilia Polian**, Univ. of Passau, Germany
Introduction by the Session Chair
- **Michael Nicolaidis**, TIMA, France
- **Mehdi B. Tahoori**, Karlsruhe Institute of Technology, Germany
Dealing with Aging Effects: A Cross-layer Approach

----- **Coffee break** -----

- **Norbert Wehn**, University of Kaiserslautern, Germany
Cross Layer Error Resilience in Wireless Communication Systems

11:30 – 12:30 ATPG

- **Nikolaus Mittermaier**, Synopsys, Germany – invited talk
Power Aware Test, a hot topic in Implementation and ATPG
- **Irih Pomeranz**, Purdue University, USA
Diagnostic Test Sets with Increased Switching Activity for Transition Faults
(research paper)

12:30 – 14:00

----- **Lunch** -----

14:00 – 14:45 Fault-Tolerance and Energy

- **Avinash Lingamneni**, CSEM, Switzerland – invited talk
Realizing Energy-Parsimonious Systems through "Inexact" Circuits
- **Sergey Frenkel**, Russian Academy of Sciences, Moscow, Russia
Some Probabilistic and Formal Techniques for Fault-Tolerant Design
(research paper)

14:45 – 15:00 Closing Remarks (A. Bystrov, P. Girard)

LPonTR'12 Chairs

Alex Bystrov, Newcastle University, UK

Patrick Girard, LIRMM, France



IEEE

IEEE  **computer society**

tttc