



Workshop on Design and Test Methodologies for Emerging Technologies

Avignon, France

May 31 – June 1, 2013

Fringe to 18th IEEE European Test Symposium

Organizers:

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Call for Papers

The workshop provides an opportunity for industry, research and academic communities to present current research and challenges encountered in their development of design and test solutions for emerging technologies. The purpose of the workshop is to update its participants on the state of the art on design and test techniques and to identify areas of recent developments that may be beneficial to participants. This will be achieved through a series of invited talks from expert speakers and through submitted papers to the workshop.

You are invited to participate in Workshop on Design and Test Methodologies for Emerging Technologies' 2013 by presenting work that focuses on design and test challenges and solution for emerging technologies in the following topics (but not limited to):

- 3D Integration
- Nanoscale and molecular scale circuits and systems
- Nanomagnetic logic and memories
- Graphene-based integrated circuits
- Carbon nanotubes circuits and systems

Submissions: Authors are invited to submit extended abstracts of 2-page maximum. All submissions will be peer-reviewed and accepted abstracts will be published in the informal proceedings of the workshop. Submissions can be emailed to

detmet_ws2013@lirmm.fr

Presentations: There will be two types of presentations, regular (30 min) and short (20 min).

Journal Publications: Best contributions will be invited for publication in Journal of *Emerging Technologies in Computing Systems (JETC)*.

Format: 2 page, IEEE conference layout, font 10, two columns, A4 paper, no page numbering, PDF file format.

Key Dates: Submission deadline: **15th April 2013**

Send to: detmet_ws2013@lirmm.fr

Notification of acceptance: 30th April 2013

Final manuscript: 11th May 2013

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