Registration/Information Hours:

Monday 25 May 2015	**12:00 - 18:30**
Tuesday 26 May 2015	**08:00 - 12:30**
	14:00 - 18:00
Wednesday 26 May 2015	**08:00 - 12:30**
Thursday 27 May 2015	**08:00 - 12:30**
	14:00 - 18:00

The Registration/Information desk will be placed in the Foyer of Grand Hotel Italia.

PROGRAM

MONDAY 25 MAY 2015

13:00-18:00	**TSS@ETS Tutorial - Erik Jan MARINISSEN (IMEC - Belgium)**
	Test and Design-for-Test of 2.5D- and 3D-Stacked Integrated Circuits

TUESDAY 26 MAY 2015

08:30-09:00	**Opening Session**
09:00-10:00	**Keynote 1 - Douglas GOODMAN (Ridgetop Group, Inc. - United States)**
	Expanding the Boundaries of Test and Diagnostics: Prognostics and Health Management (PHM) for Complex Systems Chair: Liviu MICLEA (Techical University of Cluj-Napoca - Romania)
10:00-11:00	**Poster Session and Coffee Break** Chair: Joan FIGUERAS (UPC - Spain)
	A Practical Approach for Logic Simplification Based on Fault Acceptability for Error Tolerant Application *Hideyuki ICHIHARA, Kamei JUNPEI, Tsuyoshi IWAGAKI, Tomoo INOUE (Hiroshima City Univ. - Japan)*
	Evaluating the Self-Testing Property of AES' Finite Field Inversion Units *Flavius OPRITOIU, Mircea VLADUTIU (Politehnica University of Timisoara - Romania)*
	Testing of Digital Microfluidic Biochips with Arbitrary Layouts *Trung DINH, Shigeru YAMASHITA (Ritsumeikan University - Japan), Tsung-Yi HO (National Chiao-Tung University - Taiwan), Krishnendu CHAKRABARTY (Duke University - United States)*
	Software-Based Self-Test Techniques of Computational Modules in Dual Issue Embedded Processors *Paolo BERNARDI, Riccardo CANTORO, Ernesto SANCHEZ (Politecnico di Torino - Italy), Alessandro SANSONETTI, Sergio DE LUCA, Renato MEREGALLI (STMicroelectronics - Italy), Cosimo BOVI, Davide PIUMATTI (Politecnico di Torino - Italy)*
	Reliability Analysis for Power MOSFET Based on Multi-physics Simulation *Li SHUO, Hong WANG, Yang SHIYUAN (Tsinghua University - China)*
	Session-less based Thermal-aware 3D-SIC Test Scheduling *Marie-Lise FLOTTES, Joao AZEVEDO, Giorgio DI NATALE, Bruno ROUZEYRE (LIRMM - France)*

11:00-12:30	**Session 1.1. Fault Tolerant Architectures** Chairs: Bruno ROUZEYRE (LIRMM - France), Paolo BERNARDI (Politecnico di Torino - Italy)
	An Effective Hybrid Fault-Tolerant Architecture for Pipeline Cores *Imran WALI, Arnaud VIRAZEL, Alberto BOSIO, Luigi DILILLO, Patrick GIRARD (LIRMM - France)*
	An ECC-Based Memory Architecture with Online Self-Repair Capabilities for Reliability Enhancement *Gian MAYUGA, Yuta YAMATO, Tomokazu YONEDA, Michiko INOUE (Nara Institute of Science and Technology - Japan), Yasuo SATO (Kyusyu Institute of Technology - Japan)*
	Protecting Caches Against Multi-Bit Errors Using Embedded Erasure Coding *Abbas BANAIYANMOFRAD (University of California, Irvine - United States), Mojtaba EBRAHIMI, Fabian OBORIL, Mehdi TAHOORI (Karlsruhe Institute of Technology - Germany), Nikil DUTT (University of California, Irvine - United States)*
11:00-12:30	**Session 1.2. Special Session on Biochips** Chairs: Haralampos STRATIGOPOULOS (TIMA Laboratory - France), Andrew RICHARDSON (Lancaster University - United Kingdom)
	Microfluidic Very Large Scale Integration: Technology, Fabrication and Applications *I. Emre ARACI (Stanford Microfluidics Foundry)*
	Testing of Flow-Based Microfluidic Biochips: Fault Modeling, Design-for-Testability, and Experimental Demonstration *Krishnendu CHAKRABARTY (Duke University)*
	Design Automation for Flow-Based Biochips: Fault-Tolerant Design, Error Recovery and Experimental Validation *Paul POP (Technical University of Denmark)*
11:00-12:30	**Session 1.3. Vendor Session** Chairs: Grzegorz MRUGALSKI (Mentor Graphics - Poland), Stephan EGGERSGLÜß (University of Bremen - Germany)
	At-Speed Delay Testing of Inter-Die Connections of 2.5D- and 3D-SICs *Konstantin SHIBIN (Cadence - Germany), Vivek CHICKERMANE, Brion KELLER, Christos PAPAMELETIS (Cadence - United States), Erik Jan MARINISSEN (IMEC - Belgium)*
	Scalable Test Solutions for Giga-gate Designs *Greg ALDRIC (Mentor Graphics - United States)*
	Test Solutions for Meeting Both Your Quality and Cost Goals *Rohit KAPUR (Synopsys - United States)*
12:30-14:00	**Lunch**

14:00-15:30	**Session 2.1. Functional and High Level Test** Chairs: Mounir BENABDENBI (TIMA Laboratory - France), Maksim JENIHHIN (Tallinn UT - Estonia)
	Branch Guided Functional Test Generation at the RTL *Vineeth V. ACHARYA, Sharad BAGRI, Michael S. HSIAO (Virginia Tech - United States)*
	Improving Test Pattern Generation in Presence of Unknown Values beyond Restricted Symbolic Logic *Karsten SCHEIBLER, Dominik ERB, Bernd BECKER (University of Freiburg - Germany)*
	Reliability-aware Operation Chaining in High Level Synthesis *Liang CHEN, Mojtaba EBRAHIMI, Mehdi B. TAHOORI (Karlsruhe Institute of Technology - Germany)*
14:00-15:30	**Session 2.2. ETS²: A Framework for Automation in Analog/Mixed-Signal DfT and Test – PART 1** Chairs: René SEGERS (ReSeCo - The Netherlands) and Matteo SONZA REORDA (Politecnico di Torino - Italy)
	Abstract: An AMS-test team, born during last year's ETS2, celebrates its first birthday with two sessions in Cluj. In a strong belief that action by industry was needed to enable standardization and automation in analog/mixed-signal DfT and test generation, they worked hard and are now able to present their achievements and plans at this year's ETS2. The team is eagerly asking for feedback on their proposals. These sessions should be immediately useful for those involved in analog and mixed-signal IC development, from designers and DfT specialists, to test engineers and management.
	Presentations: • Introduction to the proposal *Stephen SUNTER (Mentor Graphics)* • How to enable structural defect-oriented analog test? *Stefan VOCK (Infineon)* • Fault modeling for defect-oriented analog test *Robert VAN RIJSINGE (NXP)* • An analog test bus for standardization *Heiko AHRENS (Freescale)*
15:30-16:30	**Poster Session and Coffee Break** Chair: Sybille HELLEBRAND (University of Paderborn - Germany)
	A Low Capture Power Test Generation Method Using Capture Safe Test Vectors *Atsushi HIRAI, Toshinori HOSOKAWA, Yukari YAMAUCHI, Masayuki ARAI (Nihon University - Japan)*
	Tackling the Complexity of Exact Path Delay Fault Grading for Path Intensive Circuits *Stelios N. NEOPHYTOU (University of Nicosia - Cyprus), Maria K. MICHAEL (University of Cyprus - Cyprus)*
	Designing Area-Efficient Controllers for Multi-Cycle Transient Fault Tolerant Systems *Tsuyoshi IWAGAKI, Yutaro ISHIMORI, Hideyuki ICHIHARA, Tomoo INOUE (Hiroshima City Univ. - Japan)*
	A Soft-Error Tolerant TCAM Using Partial Don't-Care Keys *Infall SYAFALNI (Kyushu Institute of Technology - Japan), Tsutomo SASAO (Meiji University - Japan), Xiaoqing WEN, Stefan HOLST, Kohei MIYASE (Kyushu Institute of Technology - Japan)*

	Symmetric Transparent On-Line BIST of word-organized memories with Binary Adders *Ioannis VOYIATZIS (TEI of Athens - Greece)*
	A bayesian model for system level reliability estimation *Alessandro VALLERO, Alessandro SAVINO, Gianfranco POLITANO, Stefano DI CARLO (Politecnico di Torino - Italy), Sotiris TSELONIS, Nikos FOUTRIS, Manolis KALIORAKIS, Dimitris GIZOPOULOS (University of Athens - Greece),*
	A Branch-&-Bound Algorithm for TAM Optimization of Multi-Vdd SoCs *Fotios VARTZIOTIS, Xrysovalantis KAVOUSIANOS (University of Ioannina - Greece), Krishnendu CHAKRABARTY (Duke University - United States)*
16:30-18:00	**Session 3.1. Reliability and Security** Chairs: Krish CHAKRABARTY (Duke University - United States), Ondrej NOVAK (TU Liberec - Czech Republic)
	On Resistive Open Defect Detection in DRAMs: The Charge Accumulation Effect *Yiorgos SFIKAS, Yiorgos TSIATOUHAS (University of Ioannina - Greece), Mottaqiallah TAOUIL, Said HAMDIOUI (Delft University of Technology - The Netherlands)*
	Power-Aware Voltage Tuning for STT-MRAM Reliability *Elena VATAJELU (Politecnico di Torino - Italy), Rosa RODRIGUEZ-MONTANES (UPC - Spain), Stefano DI CARLO, Marco INDACO (Politecnico di Torino - Italy), Michel RENOVELL (LIRMM - France), Paolo PRINETTO (Politecnico di Torino - Italy), Joan FIGUERAS (UPC - Spain)*
	Improving RO-PUF Quality on FPGAs by Incorporating Design-Dependent Frequency Biases *Linus FEITEN, Tobias MARTIN, Matthias SAUER, Bernd BECKER (University of Freiburg - Germany)*
16:30-18:00	**Session 3.2. ETS^2: A Framework for Automation in Analog/Mixed-Signal DfT and Test – PART 2** Chairs: René SEGERS (ReSeCo - The Netherlands) and Matteo SONZA REORDA (Politecnico di Torino - Italy)
	Abstract: An AMS-test team, born during last year's ETS2, celebrates its first birthday with two sessions in Cluj. In a strong belief that action by industry was needed to enable standardization and automation in analog/mixed-signal DfT and test generation, they worked hard and are now able to present their achievements and plans at this year's ETS2. The team is eagerly asking for feedback on their proposals. These sessions should be immediately useful for those involved in analog and mixed-signal IC development, from designers and DfT specialists, to test engineers and management.
	Presentations: • Using IEEE 1687 for analog testing *Jeff REARICK (AMD), Ian HARRISON (LTX-Credence)* • Streaming digital access to ADCs and DACs *Stephen SUNTER (Mentor Graphics), Jeff REARICK (AMD)* • An example transition to 1687-based mixed-signal DfT *Peter SARSON (AMS)*

WEDNESDAY 27 MAY 2015

08:30-09:15	**Keynote 2 - Hans-Joachim WUNDERLICH (Universität Stuttgart - Germany)**
	Testing Visions Chair: Christian LANDRAULT (LIRMM - France)
09:15-10:45	**Session 4.1. Transistor Level Reliability** Chairs: Adit SINGH (Auburn University - United States), Mehdi TAHOORI (Karlsruhe Institute of Technology - Germany)
	New Drain Current Model for Nano-Meter MOS Transistors On-Chip Threshold Voltage Test *Jinbo WAN, Hans G. KERKHOFF (University of Twente - The Netherlands)*
	NBTI and Leakage Aware Sleep Transistor Design for Reliable and Energy Efficient Power Gating *Daniele ROSSI, Vasileios TENENTES (University of Southampton - United Kingdom), Saqib KHURSHEED (University of Liverpool - United Kingdom), Bashir AL-HASHIMI (University of Southampton - United Kingdom)*
	Variability-Aware Aging Modeling for Reliability Analysis of an Analog Neural Measurement System *Nils HEIDMANN, Nico HELLWEGE, Steffen PAUL, Dagmar PETERS-DROLSHAGEN (University of Bremen - Germany)*
09:15-10:45	**Session 4.2. ETS: Operational Test Issues (handling and using big data, test cell efficiency, ...)** Chairs: René SEGERS (ReSeCo - The Netherlands) and Matteo SONZA REORDA (Politecnico di Torino - Italy)
	Abstract: This session will discuss challenges in Test Operations, like how to efficiently handle, use and analyze large amounts of data through a test cell on the test floor. Introductions will be given by key industrials, including "problem owners" as well as (potential) "problem solvers".
	Presentations: • Big data and test cell efficiency *Stefan VOCK (Infineon)* • On Gaining Operational Competitiveness by Automatic Mining of 100% of the Manufacturing and Test Data - Mass Production Case Studies *Paul SIMON (Qualtera)* • Issues and opportunities in Test Operations *With contributions from NXP (Stefan EICHENBERGER) and STMicroelectronics (Davide APPELLO)*
10:45-11:15	**Coffee Break**

11:15-12:45	**Session 5.1. Analog and Mixed-Signal Test** Chairs: Sule OZEV (Arizona State University - United States), Stephane DAVID-GRIGNOT (LIRMM - France)
	Automatic Generation of Autonomous Built-In Observability Structures for Analog Circuits *Anthony COYETTE, Georges GIELEN, Esen BARIS (KU Leuven - Belgium), Wim DOBBELAERE, Ronny VANHOOREN (ON Semiconductor - Belgium)*
	Boundary cost optimization for Alternate Test *Gildas LEGER (IMSE-CNM - Spain)*
	An FPGA-based ATE Extension Module for Low-Cost Multi-GHz Memory Test *D.C. KEEZER, T.H. CHEN, T. MOON, D.T. STONECYPHER, A. CHATTERJEE (Georgia Institute of Technology - United States), H.W. CHOI, S.Y. KIM, H. YOO (Samsung Electronics Co. - Korea)*
11:15-12:45	**Session 5.2. Panel: Is Adaptive Testing the Panacea for the Future Test Problems?** Organizer: Zebo PENG (Linköping University) Moderator: Said HAMDIOUI (Technical University of Delft)
	Abstract: With the development of silicon technology and safety-critical applications, the test community is facing many new challenges. In particular, there are many emerging test problems associated with the ever-increasing process variation in the silicon manufacturing process. Adaptive testing has been proposed as a solution to many of these test problems. This panel will debate on what adaptive testing techniques can and can't do as well as the interesting problems and research issues in this area".
	Panellists: • *Erik Jan MARINISSEN, (IMEC - Belgium)* • *Peter MAXWELL (ON Semiconductor - United States)* • *Robert VAN RIJSINGE (NXP - The Netherlands)* • *Adit SINGH (Auburn University - United States)* • *Haralampos STRATIGOPOULOS (TIMA Laboratory - France)* • *Paul VAN ULSEN (Salland Engineering - The Netherlands)* • *Paul SIMON (Qualtera*
11:15-12:45	**Session 5.3. ETS: Differences and Bridges for System Level Test vs. Chip Level Test** Chairs: René SEGERS (ReSeCo - The Netherlands) and Matteo SONZA REORDA (Politecnico di Torino - Italy)
	Abstract: Today, to be able to build and test advanced and complicated electronic systems, quite some knowledge and understanding of the used semiconductor components seems to be a must. On the other hand, one can question why it would be needed to test a component again completely when it is put on a board and in a system. In this session industrial professionals will introduce board/system level test, and it's relation to testing at chip level. Together with the audience we will try to find commonalities and sharable areas in these tests. Parameters that play a role and which may be discussed include the complexity of the IC/board/system, the application, the design, standards and tools. The goal of the session is to find approaches and options so that all tests in the system supply

	chain can be accomplished more efficiently and with a high quality. We invite IC/board/system designers and specifically test and product engineers to join the discussion!
	Presentations: • *Xinli GU (Huawei Technologies)* • *Jun QIAN (AMD)* • *Martin KEIM (Mentor Graphics)* • *Peter VAN DEN EIJNDEN (JTAG Technologies)*
12:45-14:00	**Lunch**
14:00-15:00	**Session 6.1. Embedded tutorial: Industrial Advancements in Diagnosis Driven Yield Analysis** Yu HUANG, Wu-Tung CHENG, Wu YANG (Mentor Graphics - United States) Chair: Alberto BOSIO (LIRMM - France)
	Abstract: Delivering a stable high yield product on time is the ultimate goal for the semiconductor industry. Reaching this goal becomes more and more difficult, especially when diagnosing cell internal defects and back-end-of-line (BEOL) defects becomes critical. Too often, the yield is lower than expected or takes longer to ramp to the target level. One of the main challenges in the yield analysis process is to identify the systematic issue, find its root cause and select associated devices for failure analysis. Furthermore, it is very important to find the right die candidate for physical failure analysis (PFA) and provide enough information about the selected suspects to reduce the time consuming and expensive PFA efforts. This embedded tutorial discusses the methodologies that improve yield of digital semiconductor devices through scan-based test and volume diagnosis driven yield analysis (DDYA). Scan chain diagnosis and layout-aware logic diagnosis can provide fast and accurate volume diagnosis results and subsequent statistical analysis can provide the technologies to carry out this methodology. This gives failure analysis engineers and yield engineers a very fast and highly effective way of defect localization and identification, complementing their traditional, hardware-based methods.
14:00-15:00	**Session 6.2. Embedded tutorial: Testing of Analog/Mixed Signal ICs: Past, Present and Future** Bram KRUSEMAN (NXP Semiconductors) Chair: Jochen RIVOIR (Advantest - Germany)
	Abstract: Testing of Analogue/Mixed Signal ICs has reached a transition point. In the past AMS testing was based on functional tests that ensured that the analogue specifications were met. Unfortunately this approach is expensive; testing an 'analogue' transistor can be 1000x more expensive than testing a digital transistor. What is even a bigger concern in industry is that a large fraction of the AMS test development takes place after first silicon. Digital blocks are up and running in hours while the AMS part typically takes days or weeks. As a result AMS test is in the critical path towards the customer. Hence, the specification-based functional-test approach is becoming very costly both from a test time point of view and from a test development point of view. Already for a number of years industry is exploring alternatives. In the tutorial a number of those alternatives are covered such as usages of DC measurements instead of dynamic measurements, BIST for AMS blocks, and structural test approaches. These approaches have the advantage that they enable shorter test times but also that it can be verified before tape-out, hence shifting the effort out of the critical path. The tutorial is concluded with an outlook on the future requirements that address a frame-work for fast verification, validation and characterization of AMS blocks and test requirements related to adaptive AMS blocks which adjust

	their performance over lifetime.
14:00-15:00	**Session 6.3. Embedded tutorial: FinFET Technology and its impact on memory test & repair** Yervant ZORIAN (Synopsys)
	Abstract: FinFET transistors are playing an important role in modern technology that is rapidly growing. Embedded memories based on FinFET transistors lead to new defects that can require new embedded test and repair solution. To investigate FinFET-specific faults the existing models and detection techniques are not enough due to a special structure of FinFET transistors. This embedded tutorial discusses a new approach for investigation of FinFET-specific faults. In addition to fault modeling, a new methodology is presented for test & repair algorithm generation. This methodology has been validated on several real FinFET-based embedded memory technologies down to 10nm.

THURSDAY 28 MAY 2015

08:30-10:00	**Session 7.1. High Frequency and RF** Chairs: Gildas LEGER (IMSE-CNM - Spain), Hans KERKHOFF (University of Twente - The Netherlands)
	High Frequency Jitter Estimator for SoCs *Herve LE GALL (STMicroelectronics - France), Rshdee ALHAKIM, Miroslav VALKA, Salvador MIR, Haralampos STRATIGOPOULOS, Emmanuel SIMEU (TIMA Laboratory - France)*
	A New Technique for Low-Cost Phase Noise Production Testing from 1-bit Signal Acquisition *Stephane DAVID-GRIGNOT, Florence AZAIS, Laurent LATORRE (LIRMM - France), Francois LEFEVRE (NXP, FR - France)*
	Robust Amplitude Measurement for RF BIST Applications *Jae Woong JEONG, Jennifer KITCHEN, Sule OZEV (Arizona State University - United States)*
08:30-10:00	**Session 7.2. Special session on Security of CPS and IoT** Chairs: Said HAMDIOUI (Delft University of Technology - The Netherlands), Ilia POLIAN (University of Passau - Germany)
	Cybersecurity for the smart-grid: Manhattan Case Study *Michail MANIATAKOS (NYU Abu Dhabi)*
	Cross-Layer Protection on Cyber-Physical System *Yier JIN (University of Central Florida)*
	PUFs for Embedded Hardware Security: Delay Based PUF for Smart Devices *Fareena SAQIB (Florida Institute of Technology)*
08:30-09:30	**Session 7.3. Vendor Session** Chair: Ioan STOIAN (IPA Cluj - Romania)
	Process Safety in Off-Shore Deep Sea Oil Extraction *Mihai DABOC, Andras ZOR (ARQES - Romania)*
	FPGA Instrumentation - New trends in automated test

	Vlad ZILERIU, Horia HEDESIU (National Instruments - Romania)
10:00-11:00	**Poster Session and Coffee Break** Chair: Jose Luis HUERTAS DIAZ (IMSE-CNM - Spain)
	A Fault Tolerant Response Analyzer with Self-Error-Correction Capability *Yuki FUKAZAWA (Mie University - Japan), Hideyuki ICHIHARA, Tomoo INOUE (Hiroshima City Univ. - Japan)*
	LSI Aging Estimation Using Ring Oscillators *Yukiya MIURA, Tatsunori IKEDA (Tokyo Metropolitan Univ. - Japan)*
	Software-based Repair for Memories in Tiny Embedded Systems *Mario SCHOELZEL, Patryk SKONCEJ (IHP (Frankfurt/Oder) - Germany)*
	Efficient Diagnosis Technique for Aging Defects on Automotive Semiconductor Chips *Jihun JUNG, Muhammad Adil ANSARI, Dooyoung KIM (Hanyang University - Korea), Hyunbean YI (Hanbat University - Korea), Sungju PARK (Hanyang University - Korea)*
	Re-using BIST for Circuit Aging Monitoring *Farshad FIROUZI (KIT - Germany), Fangming YE (Duke University - United States), Arunkumar VIJAYAN (KIT - Germany), Abhishek KONERU, Krishnendu CHAKRABARTY (Duke University - United States), Mehdi B. TAHOORI (KIT - Germany)*
11:00-12:30	**Session 8.1. Compression** Chairs: Jerzy TYSZER (Poznan University of Technology - Poland), Peter WOHL (Synopsys - United States)
	Compact Test Set Generation for Test Compression-based Designs *Stephan EGGERSGLUESS (University of Bremen - Germany)*
	Improve the Compression Ratios for Code-Based Test Vector Compression by Decomposing *Jishun KUANG, Liang ZHANG, Zhiqiang YOU, Yingbo ZHOU (Hunan University - China)*
	On Test Program Compaction *Marco GAUDESI, Matteo SONZA REORDA (Politecnico Di Torino - Italy), Irith POMERANZ (Purdue University - United States)*
11:00-12:30	**Session 8.2. Panel: Analog Test: Why still "à la mode" after more than 25 years of research?** Organizer: Florence AZAIS (LIRMM - France) Moderator: Salvador MIR (TIMA - France)
	Abstract: Test of analog, mixed-signal and RF circuits has been a topic of active research for more than 25 years and many ideas presented at conferences and published in journals. Despite this strong activity, it is still a hot topic that attracts many submissions in major test conferences. Does it means that all ideas proposed so far are useless or does it means that the domain is in constant evolution and that new challenges arise which necessitate novel ideas? Panelists both from industry and academia, all experts in the domain, will present their arguments on the reason for longevity of the analog test topic and will give their view on the future of this topic, if any…

	Panellists: • *Steve SUNTER (Mentor Graphics - Canada)* • *Peter SARSON (AMS - Austria)* • *Hans HERKHOFF (University of Twente - The Netherlands)* • *Marco SPINETTA (STM - Italy)* • *Sule OZEV (ASU - United States)*
11:00-12:30	**Session 8.3. Vendor Session** Chairs: Szilard ENYEDI (Technical University of Cluj-Napoca - Romania), Ioannis VOYIATZIS (TEI of Athens - Greece)
	Advancements in field of test circuits for testing performance, timing and power of memory IPs *Anand K. BALAN (ARM - India), Joonsoo PARK (ARM - United States), Neha AGARWAL (ARM - India), Faisal KHOJA (ARM - United States), Ramesh MANOHAR, Sagar UNDALE (ARM - India), Rupal GANDHI (ARM - United States)*
	Testing Inside & Outside *Hans MANHAEVE (Ridgetop - Belgium)*
	Automated Testing of Bare Die-to-Die Stacks *Erik Jan MARINISSEN, Bart de WACHTER, Teng WANG (IMEC - Belgium), Jens FIEDLER, Joerg KIESEWETTER, Karsten STOLL (Cascade Microtech GmbH)*
12:30-14:00	**Lunch**
14:00-15:30	**Session 9.1. Power and Reliability** Chairs: Stefano DI CARLO (Politecnico di Torino - Italy), Peter MAXWELL (ON Semiconductor - United States)
	Identification of High Power Consuming Areas with Gate Type and Logic Level Information *Kohei MIYASE (Kyushu Institute of Technology - Japan), Matthias SAUER, Bernd BECKER (University of Freiburg - Germany), Xiaoqing WEN, Seiji KAJIHARA (Kyushu Institute of Technology - Japan)*
	Diagnosis of Power Switches with Power-Distribution-Network Consideration *Vasileios TENENTES, Daniele ROSSI, Bashir AL-HASHIMI (University of Southampton - United Kingdom), Saqib KHURSHEED (University of Liverpool - United Kingdom)*
	Aging Guardband Reduction through Selective Flip-Flop Optimization *Mohammad Saber GOLANBARI, Saman KIAMEHR, Mojtaba EBRAHIMI, Mehdi B. TAHOORI (KIT - Germany)*
15:30-16:00	**Closing Session**