ETS 2016 Program

Registration/Information Hours

ETS	**Registration desk at Foyer I**
Monday 23 May	12:00-18:30
Tuesday 24 May	08:00-18:30
Wednesday 25 May	08:00-15:00
Thursday 26 May	08:00-16:00
Workshop	**Registration desk at Meeting Centre 2**
Thursday 26 May	16:00-18:00
Friday 27 May	08:00-08:30

Monday May 23th, 2016

14:00-17:30 TSS@ETS Tutorials

The TSS Tutorials of Monday afternoon are accessible to all ETS attendees with a Full Registration. The complete TSS program can be found here.

- **14:00-15:30 Combining Structural and Functional Test Approaches Across System Levels: IC Test**
  Matteo Sonza Reorda (Politechnico di Torino - Italy)
- **15:30-16:00 Break**
- **16:00-17:30 Combining Structural and Functional Test Approaches Across System Levels: Board Test**
  Artur Jutman (Testonica - Estonia)

19:00-20:30 Welcome Reception

Tuesday May 24th, 2016

08:30-09:00 Opening

09:00-10:00 Keynote 1

Chair: Hans-Joachim Wunderlich (University of Stuttgart, DE)

- **Securely Connected Vehicles – What it takes to make self-driving cars a reality**
  Lars Reger, CTO Automotive, NXP Semiconductors, Hamburg, Germany

10:00-11:00 Coffee Break, Poster Session 1 and Table-Top Demos

Chair: Ilia Polian (University of Passau, DE)

- **Compressor design for silicon debug**
  Jing ZHANG (Lund University - Sweden), Lars Johan FRITZ (Ericsson - Sweden), Liang LIU, Erik LARSSON (Lund University - Sweden)
- **An optical/electrical test system for 100Gb/s optical interconnection devices with high volume testing capability**
  Tasuku FUJIBE, Kazuki SHIRAHATA, Takeshi MIZUSHIMA, Hidenobu MATSUMURA, Daisuke WATANABE, Hiroyuki MINEO, Shin MASUDA (Advantest Laboratories - Japan)
- **CPE: Codeword Prediction Encoder**
  Satish GRANDHI (UCC - Ireland), Elsa DUPRAZ (Telecom Bretagne - France), Christian SPAGNOL (University College Cork - Ireland), Valentin SAVIN (CEA-LETI - France), Emanuel POPOVICI (University College Cork - Ireland)
- **Reliability Enhancement of Embedded Memory with Combination of Aging-aware Adaptive In-Field Self-Repair and ECC**
  Gian MAYUGA, Yuta YAMATO, Tomokazu YONEDA (Nara Institute of Science and Technology - Japan), Yasuo SATO (Kyusyu Institute of Technology - Japan), MICHIKO INOUE (Nara Institute of Science and Technology - Japan)
- **In situ Measurement of Aging–induced Performance Degradation in Digital Circuits**
  Nasim POUR ARYAN, Christian FUNKE, Jens BARGFREDE (Infineon Technologies AG - Germany), Cenk Yilmaz, Doris Schmitt-Landsiedel (Technical University of Munich - Germany), Georg Georgakos (Infineon Technologies AG - Germany)
- **A Novel Threshold Defined Switch for Circuit Camouflaging**
  Ithihasa Reddy NIRMALA, Deepak Reddy VONTELA, Swaroop GHOSH, Anirudh IYENGAR (University of Southflorida - United States)
- **Study of a Delayed Single-Event Effect in the Muller C-element**
  Varadan SAVULIMEDU VEERAVALLI, Andreas STEININGER (TU Vienna - Austria)

Table-Top Demos

- **Technoprobe Wafer Sort Probing Solution**
  Alessandro Antonioli, Raffaele Vallauri (Technoprobe - Italy)
- **Benchtop debug and characterization of ATPG test patterns and IJTAG instruments**
  Geir Eide, Givargis Danialy (Mentor Graphics - United States)
- **Ridgetop Solutions for Process and device qualification and reliability assessment**
  Hans Manhaeve, Craig Wentzel (Ridgetop Europe - Belgium)

11:00-12:30 Session 1

11:00-12:30 1A: Reliability, Fault Tolerance and Security

Chairs: Subhasish Mitra (Stanford University, US) and Imran Wali (LIRMM, FR)

- **A Self-Reconfiguring IEEE 1687 Network for Fault Monitoring**
  Farrokh GHANI ZADEGAN, Dimitar NIKOLOV, Erik LARSSON (Lund University - Sweden)
- **Addressing Transient Routing Errors in Fault- Tolerant Networks-on-Chips**
  Amir CHARIF, Nacer-Eddine ZERGAINOH, Michael NICOLAIDIS (TIMA Laboratory - France)
- **Formal Verification of Secure Reconfigurable Scan Network Infrastructure**
  Michael KOCHTE, Rafal BARANOWSKI (University of Stuttgart - Germany), Matthias SAUER, Bernd BECKER (University of Freiburg - Germany), Hans-Joachim WUNDERLICH (Universitat Stuttgart - Germany)

11:00-12:30 1B: Vendor - Advances in Probe Technology

Chair: Jochen Rivoir (Advantest, DE)

- **Advanced Probe-Card Technologies**
  Joe MAI (JEM Europe - France)
- **Ultra-fine pitch probing challenges and solutions**
  Raffaele VALLAURI (Technoprobe - Italy), Erik Jan MARINISSEN (IMEC - Belgium), Alessandro ANTONIOLI, Marco PREA, Daniele ACCONCIA (Technoprobe - Italy)
- **A Full-Automatic Test System for Direct Probing of JEDEC Wide-I/O Micro-Bumps**
  Mireille Matterne, Bart De Wachter, Ferenc Fodor, Erik Jan Marinissen (IMEC, Belgium); Joerg Kiesewetter, Mario Berg, Torsten Kern (Cascade Microtech GmbH, Germany); Ken Smith, Eric Hill (Cascade Microtech Inc., USA)

11:00-12:30 1C: ETS^2 - A framework for automation in analog/mixed-signal DfT and test

Chairs: René Segers (ReSeCo, NL) and Matteo Sonza Reorda (Politecnico di Torino, IT)

An AMS-test team was born during ETS^2 in 2014, in a strong belief that action by industry was needed to enable standardization and automation in analog/mixed-signal DfT and test generation. They have been meeting bi-weekly since then, presented some results for ETS audience input in 2015, and now have a draft document with proposed rules to summarize at this year's ETS^2, along with an update on their parallel draft standard for analog fault simulation and publicly releasable analog benchmarks. The team is eager to hear feedback. This session should be immediately useful for those involved in analog and mixed-signal IC development, from designers and DfT specialists, to test engineers and management.

- **A structured DfT approach for analog test bus connections**
  Hans Martin von Staudt (Dialog Semiconductors, Germany)
- **Standardizing descriptions and rules for analog DfT circuitry using IEEE 1687**
  Jeff Rearick (AMD, USA)
- **Update on development of a standard for analog fault modeling and simulation**
  Stephen Sunter (Mentor Graphics, USA)

12:30-14:00 Lunch

14:00-15:30 Session 2

14:00-15:30 2A: Delay Testing in 3D ICs

Chairs: Maria Michael (Cyprus University, CY) and Mottaqiallah Taouil (Technical University of Delft, NL)

- **Testing of Small Delay Faults in a Clock Network**
  Shao-fu YANG(National Tsing Hua U. - Taiwan), Shi-Yu HUANG (National Tsing-Hua University - Taiwan), Kun-Han TSAI (Mentor Graphics - United States), Wu-Tung CHENG (Mentor Graphics Corporation - United States)
- **Analysis of Electrostatic Coupling in Monolithic 3D Integrated Circuits and its Impact on Delay Testing**
  Abhishek KONERU, Krishnendu CHAKRABARTY (Duke University - United States)
- **A Built-In Method for Measuring the Delay of TSVs in 3D ICs**
  Han-Yu WU, Yong-Xiao CHEN, JIN-FU LI (National Central University - Taiwan)

14:00-15:30 2B: VENDOR - EDA FOR AUTOMOTIVE APPLICATIONS

Chair: Pete Harrod (ARM, UK)

- **Ethernet Verification IP for Automotive Applications – Facilitating ISO 26262**
  Daniel BAYER (Cadence Design Systems - Germany)
- **Test Solutions for Automotive Designs**
  Geir EIDE (Mentor Graphics - United States)
- **ISO 26262-Certified Solution for Testing of Safety-Critical Automotive ICs**
  Rohit KAPUR (Synopsys Inc. - United States)

14:00-15:30 2C: ETS² - TEST SUPPORTING A PRODUCT LAUNCH AT ENTITLEMENT YIELD

Chairs: René Segers (ReSeCo, NL) and Matteo Sonza Reorda (Politecnico di Torino, IT)

In an ever faster turning world, it is essential to launch new devices right at defectivity limited yield, no matter whether they are analog, digital, mixed signal, and contain RAM, ROM, Flash or other more exotic parts. In order to achieve this, maybe one need to do things to a wafer that no simulation can predict. By stretching Vdd, temperature, frequency outside of normal regions we can evaluate stability and margins prior to ramp. Is this extensive "teasing" the only way to achieve entitlement yield quickly? This session is all about how to boost the learning cycle at product launch and which role Test can/should play. We conclude again that Test is much more than "just" detecting faults, and discusses the emerging challenges and opportunities of Test, specifically in the field of Yield learning and Yield Improvement. Please join the discussions, your participation is highly appreciated!

- **Test it to Break it**
  Jeff Roehr (Texas Instruments, USA)
- **Test Experiences in Targeting Entitlement Yield**
  Stefan Eichenberger (NXP, Germany/The Netherlands)

15:30-16:30 Coffee Break, Poster Session 2 and Table-Top Demos

Chair: Alberto Bosio (LIRMM, FR)

- **On the Diagnostic Analysis of IEEE 1687 Networks**
  Riccardo CANTORO, Mehrdad MONTAZERI, Matteo SONZA REORDA (Politecnico di Torino - Italy), Farrokh GHANI ZADEGAN, Erik LARSSON (Lund University - Sweden)
- **On Coverage of Timing Related Faults at Board Level**
  Artur JUTMAN (Testonica Lab - Estonia), Igor ALEKSEJEV (Tallinn University of Technology - Estonia), Sergei DEVADZE (Tallinn University of Technology - Estonia)
- **A Low-cost Susceptibility Analysis Methodology to Selectively Harden Logic Circuits**

Imran WALI, Bastien DEVEAUTOUR, Arnaud VIRAZEL, Alberto BOSIO, Patrick GIRARD (LIRMM - France), Matteo SONZA REORDA (Politecnico Di Torino - Italy)

- **A 40Gbps Economic Extension Board and FPGA-based Testing Platform**
  Te-Hui CHEN, David KEEZER (Georgia Institute of Technology - United States)
- **Combining the Histogram Method and the Ultrafast Segmented Model Identification of Linearity Errors Algorithm for ADC Linearity Testing**
  Weida CHEN, Yongxin ZHU (Shanghai Jiao Tong University - China), , Xinyi LIU, Xinyang LI (Shanghai Jiao Tong University - China), Dongyu OU (Texas Instruments Semiconductor Technologies (Shanghai) Co., Ltd. - China)
- **A Scheduling Method for Hierarchical Testability Based on Test Environment Generation Results**
  Jun NISHIMAKI, Toshinori HOSOKAWA (Nihon University - Japan), Hideo FUJIWARA (Osaka Gakuin University - Japan)
- **The Influence of Hysteresis Voltage on Single Event Transients in a 65nm CMOS High Speed Comparator**
  Illani MOHD NAWI, Basel HALAK, Mark ZWOLINSKI (University of Southampton - United Kingdom)

16:30-18:00 Session 3

16:30-18:00 3A: Test Vectors and Standards

Chairs: Jerzy Tyszer (Poznan University of Technology, PL) and Zebo Peng (Linköping University, SE)

- **Analysis and Design of an On-Chip Retargeting Engine for IEEE 1687 Networks**
  Ahmed IBRAHIM, Hans KERKHOFF (University of Twente - Netherlands)
- **A Novel Test Generation and Application Flow for Functional Access to IEEE 1687 instruments**
  Michele PORTOLAN (TIMA - France)
- **VecTHOR: Low-cost compression architecture for IEEE 1149-compliant TAP controllers**
  Sebastian HUHN, Stephan EGGERSGLUESS, Rolf DRECHSLER (University of Bremen - Germany)

16:30-18:00 3B: Vendor - Mixed-Signal and RF Test

Chair: Haralampos Stratigopoulos (LIP6, FR)

- **Augmenting Testability in Mixed-signal SerDes IP through IEEE 1687-Compliant DFT Ecosystem**
  Vladimir ZIVKOVIC (Cadence - United Kingdom), John VOGEL (Cadence Design Systems - United States), Rajesh KHURANA (Cadence Design Systems - India), Scott SHELTON, Daniel COHEN (Cadence Design Systems - United States), Colin SCOTT (Cadence Design Systems - United Kingdom), Vivek CHICKERMANE, Krishna CHAKRAVADHANULA (Cadence Design Systems - United States)
- **ATPG tool for Automotive and Mixed Signal Test**
  Frans MOSSELVELD (Xcerra Corporation - Germany), Piet-Jan KROMWIJK (NXP - Netherlands)
- **When normal ATE is not enough...RF testing above 6 GHz**
  Rien VAN OORD, Paul VAN ULSEN (Salland Engineering - Netherlands)

16:30-18:00 3C: ETS² - How chip level testing correlates to system level testing and quality, and vice versa

Chairs: René Segers (ReSeCo, NL) and Matteo Sonza Reorda (Politecnico di Torino, IT)

Even with a 100% structural IC test there may still be remaining undetected defects or even design errors. Detecting and localizing these marginal defects or errors is a most challenging job. At the system level it may require the system running in a customer field with their applications, while structurally a huge pile of structural system data may have to be analyzed and be linked back to IC level test data. At the IC level it remains a huge challenge to achieve a 100% coverage. Besides, hampering issues may include that structural test approaches are not enabled under the functional test and, in many cases, one cannot even guarantee to reproduce the customer applications, caused by "intermittent" errors and leading to NTF (No Trouble Found). Hence, new test and analysis technologies need to be explored, while innovative DfX (Design for ...) means and methods are urgently demanded for complicated systems such that root-causes can be found quickly. The session discusses experiences both from the chip perspective as well from the system level, and hence should be attractive for almost all ETS attendees. You are all invited to take part in the discussions.

- **What do you want to get from system failure for chip FA and do you know how hard this is?**
  Xinli Gu (Huawei Technologies, USA)
- **Exposing marginal defects by non-destructive stress testing**
  Harry Chen (Mediatek, Taiwan)
- **Case Studies of Marginal Failures that Escaped Chip-level Structural Tests**
  Phil Nigh (GLOBALFOUNDRIES, USA)

18:15-20:00 Cheese and Wine Panel

Wednesday May 25th, 2016

08:30-09:30 Keynote 2

Chair: Erik Jan Marinissen (IMEC, BE)

- **Is IoT Coming to the Rescue of Semiconductor?**
  Cheng-Wen Wu, Department of Electrical Engineering, National Tsing Hua University (NTHU), Hsinchu, Taiwan

09:30-10:30 Session 4

09:30-10:30 4A: Emerging Technologies

Chairs: Elena Ioana Vatajelu (Politecnico di Torino, IT) and Matthias Sauer (University of Freiburg, DE)

- **Behavior and Test of Open-Gate Defects in FinFET Based Cells**
  Francisco MESALLES (National Institute for Astrophysics, Optics and Electronics - Mexico), Hector VILLACORTA (Polytechnic University of Aguascalientes - Mexico), Michel RENOVELL (Universite de Montpellier - France), Victor CHAMPAC (INAOE - Mexico)
- **Test-station development for semi-automatic wafer-level silicon photonics platform testing**
  Jeroen DE COSTER, Peter DE HEYN, Marianna PANTOUVAKI, Brad SNYDER, Hongtao CHEN, Erik Jan MARINISSEN, Philippe ABSIL, Joris VAN CAMPENHOUT (IMEC - Belgium), Bryan Bolt (Cascade Microtech Inc., USA)

09:30-10:30 4B: Analog Test

Chairs: Wim Dobbelaere (ON Semiconductor, BE) and Hans Kerkhoff (University of Twente, NL)

- **Questioning the reliability of Monte Carlo simulation for machine learning test validation**
  Gildas LEGER (IMSE-CNM - Spain), Manuel BARRAGAN (TIMA Laboratory - France)
- **Linearity Test of High-speed High-performance ADCs using a Self-Testable On-chip Generator**
  Antonio GINES (IMSE-CNM (CSIC, Universidad de Sevilla) - Spain), Eduardo PERALIAS (Instituto de Microelectronica de Sevilla (IMSE-CNM) - Spain), Adoracion RUEDA (IMSE-CNM, USE - Spain), Gildas LEGER (IMSE-CNM - Spain), Guillaume RENAUD, Manuel BARRAGAN, Salvador MIR (TIMA Laboratory - France)

09:30-10:30 4C: Embedded Tutorial

Chair: Paolo Bernardi (Politecnico di Torino, IT)

- **Automotive embedded software architecture in the multicore age**
  Massimo VIOLANTE (Politecnico di Torino - Italy), Paolo GAI (Evidence - Italy)

10:30-11:00 Coffee Break and Table-Top Demos

11:00-12:30 Session 5

11:00-12:30 5A: Test and DfT for 3D ICs

Chairs: Saqib Khursheed (University of Liverpool, UK) and Mounir Benabdenbi (TIMA, FR)

- **IJTAG supported 3D DFT using Chiplet-Footprints for testing Multi-Chips Active Interposer System**
  Jean DURUPT, Pascal VIVET (CEA - France), Juergen SCHLOEFFEL (Mentor Graphics Development (Deutschland) GmbH - Germany)
- **A Design-for-Test Solution for Monolithic 3D Integrated Circuits**
  Ran WANG, Krishnendu CHAKRABARTY (Duke University - United States)
- **Two-Dimensional Time-Division Multiplexing for 3D-SoCs**
  Panagiotis GEORGIOU, Fotios VARTZIOTIS, Xrysovalantis KAVOUSIANOS (University of Ioannina - Greece), Krishnendu CHAKRABARTY (Duke University - United States)

11:00-12:30 5B: Vendor - Embedded Instruments and (I)JTAG

Chair: Janusz Rajski (Mentor Graphics, US)

- **Online LBIST Requirements and Recommendations for an ARM® Multicore Processor**
  Teresa MCLAURIN (ARM - United States)
- **The Need for Chip-Embedded Test Provisions for Board-level Testing**
  Peter VAN DEN EIJNDEN, Anne-Marie VAN DEN HURK (JTAG Technologies - Netherlands)
- **The Odds of Test and Measurement**
  Hans MANHAEVE (Ridgetop Europe - Belgium)

11:00-12:30 5C: Diagnosis & Silicon Debugging

Chairs: Bram Kruseman (NXP Semiconductors, NL) and Michel Renovell (LIRMM, FR)

- **Cell-Aware Diagnosis: Defective Inmates Exposed in their Cells**
  Peter MAXWELL (ON Semiconductor - United States), Friedrich HAPKE (Mentor Graphics - Germany), Huaxing TANG (Mentor Graphics - United States)
- **A Fast Sweep-Line-Based Failure Pattern Extractor for Memory Diagnosis**
  Sin-Yu WEI (National Tsing Hua University - Taiwan), Bing-Yang LIN (NTHU - Taiwan), Cheng-Wen WU (National Tsing Hua University - Taiwan)
- **Bit-flip Detection-Driven Selection of Trace Signals**
  Amin VALI (McMaster Univ - Canada), Nicola NICOLICI (McMaster University - Canada)

12:30-14:00 Lunch

14:00-15:00 Session 6: Embedded Tutorials

14:00-15:00 6A: Embedded Tutorial

Chair: Liviu Miclea (Technical University of Cluj-Napoca, RO)

- **Cell Aware and Stuck-Open Tests**
  Adit SINGH (Auburn University - United States)

14:00-15:00 6B: Embedded Tutorial

Chair: Pascal Vivet (CEA-Leti, FR)

- **Practices in High Speed I/O Testing**
  Salem ABDENNADHER (Intel Corporation - United States), Saghir SHAIKH (Broadcom - United States)

14:00-15:00 6C: EMBEDDED TUTORIAL

Chair: Lorena Anghel (TIMA, FR)

- **Cross-Layer Resilience**
  Subhasish MITRA (Stanford University - United States)

15:00-22:30 Social Event

Thursday May 26th, 2016

09:00-10:00 Keynote 3

Chair: Adit Singh (Auburn University, US)

- **Testing in the Year 2024 – Big Changes are Coming**
  Phil Nigh, GlobalFoundries, USA

10:00-11:00 Coffee Break and Poster Session 3

Chair: Patrick Girard (LIRMM, FR)

- **Measuring Defect Tolerance within Mixed-Signal ICs**
  Stephen SUNTER (Mentor Graphics - Canada), Alessandro VALERIO, Riccardo MIGLIERINA (ST Microelectronics - Italy)
- **Group delay filter measurement using a chirp**
  Peter SARSON (ams AG - Austria)
- **Component Fault Localization using Switching Current Measurements**
  Seetal POTLURI (IIT Madras - India), A. Satya TRINADH (IIT Hyderabad - India), Siddhant SARAF, Kamakoti VEEZHINATHAN (IIT Madras - India)
- **A new EDA flow for the Mitigation of SEUs in Dynamic Reconfigurable FPGAs**
  Boyang DU, Luca STERPONE (Politecnico di Torino - Italy), David Merodio CODINACHS (European Space Agency - Netherlands)
- **Failure Mechanisms and Test Methods for the SRAM TVC Write-Assist Technique**
  Josef KINSEHER, Moritz VOLKER (Intel Mobile Communications - Germany), Leonardo ZORDAN (Intel Mobile Communications - France), Ilia POLIAN (University of Passau - Germany)
- **Read Path Degradation Analysis in SRAM**
  Innocent AGBO (TU Delft - Netherlands), Mottaqiallah TAOUIL, Said HAMDIOUI (Delft University of Technology - Netherlands), Pieter WECKX, Stefan COSEMANS, Francky CATTHOOR (Imec Belgium - Belgium), Wim DEHAENE (KU Leuven Belgium - Belgium)
- **A Hybrid Algorithm to Conservatively Check the Robustness of Circuits**
  Niels THOLE (University Bremen - Germany), Lorena ANGHEL (Grenoble-Alpes University, TIMA Laboratory - France), Görschwin FEY (University of Bremen / DLR - Germany)

11:00-12:30 Session 7

11:00-12:30 7A: Test Generation

Chairs: Peter Maxwell (ON Semiconductor, US) and Michael Kochte (University of Stuttgart, DE)

- **SAT-Based Post-Processing for Regional Capture Power Reduction in At-Speed Scan Test Generation**
  Stephan EGGERSGLUESS (University of Bremen - Germany), Kohei MIYASE, Xiaoqing WEN (Kyushu Institute of Technology - Japan)
- **Utilizing Shared Memory Multi-cores to Speed-up the ATPG process**
  Stavros HADJITHEOPHANOUS (University of Cyprus - Cyprus), Stelios NEOPHYTOU (University of Nicosia - Cyprus), Maria MICHAEL (University of Cyprus - Cyprus)

- **Transistor Stuck-on Fault Detection Tests for Digital CMOS Circuits**
  Xijiang LIN (Mentor Graphics Corp. - United States), Sudhakar REDDY (University of Iowa - United States), Janusz RAJSKI (Mentor Graphics Corporation - USA)

11:00-12:30 7B: VENDOR - HIGH-VOLUME MANUFACTURING AND TEST

Chair: Grzegorz Mrugalski (Mentor Graphics, US)

- **Leveraging Extreme Analytics to Identify and Prevent Outliers in High-Volume Semiconductor Manufacturing**
  David PARK (Optimal Plus - United States), Gil LEVY, Dan SEBBAN (Optimal Plus - Israel), Marco ESPOSITO (Optima Plus - Italy)
- **Big Data Analytics Innovations for Gaining Operational Excellence in Test and Manufacturing**
  Paul SIMON (Qualtera - France)
- **Silicon Photonics optical and electrical wafer probing**
  Paul MOONEY (Tokyo Electron Europe Ltd. - United Kingdom)

11:00-12:30 7C: SPECIAL SESSION: IEEE STD P1838: DFT STANDARD-UNDER-DEVELOPMENT FOR 2.5D-, 3D, AND 5.5D-SICS

Organizer: Erik Jan Marinissen (IMEC, Belgium) - IEEE P1838 Founder and Chair

Moderator: Michael Wahl (University of Siegen, Germany) - IEEE P1838 Editor

Now that conventional technology scaling is becoming harder and costlier, the momentum of Moore's Law will be propped up by vertical stacking of integrated circuits. There are both 2.5D and 3D stacking methodologies. In 2.5D-SICs, multiple active dies are placed side-by-side on top of and interconnected by a passive interposer die. In 3D-SICs, multiple active dies are stacked vertically. Both 2.5D- and 3D-SICs are enabled by the capability to manufacture through-silicon vias (TSVs) that provide an electrical connection between the front- and back-side of a silicon substrate and high-density micro-bumps. In 2.5D-SICs, TSVs connect the stacked active dies through the silicon interposer to the package substrate. In 3D-SICs, TSVs provide vertical interconnections between the various stacked dies. The TSVs, micro-bumps, and interposer wires provide inter-die connections that, compared to traditional inter-die interconnect, offer high bandwidth at low power consumption. Both types of SICs serve their particular market segments and are here to stay; 2.5D-SICs provide better chip cooling options and hence typically target high-performance computing and networking applications, whereas 3D-SICs with their small footprint are better suited for mobile applications.
Like all micro-electronic products, these SICs need to be tested for manufacturing defects. Testing requires test access, achieved by on-chip design-for-test (DfT) features. For 2.5D- and 3D-SICs, where the final product consists of multiple interconnected dies, effective test access requires the DfT features in the various dies to operate in a concerted way. For example: tester access is through the external chip I/Os that typically reside in the bottom die; testing the top die in the stack requires a collaborative effort from the DfT in the lower die(s) to elevate the test stimuli up and the test responses down through the stack. This 3D-DfT can be proprietary if all dies in the stack are made by a single company. However, in the likely case that the various dies in the stack originate from different companies, standardized 3D-DfT is required to guarantee a minimum of inter-operability. IEEE Std P1838 is a standard-under-development that addresses exactly this issue.
The P1838 Working Group started its work in 2011. Consisting of around 50 test professionals, representing a cross-section of the industry, this team has been working diligently to identify the requirements for a 3D-DfT standard, to define the 3D-DfT architecture, and to specify detailed rules, permissions, and recommendations. The standardization process is not completed yet! However, in this Special Session, three active members of the P1838 Working Group present their views of the three main components

(the serial control mechanism, the die wrapper register, and the flexible parallel port) of the standard-under-development to the ETS audience.

- **IEEE Std P1838 Introduction and Serial Control Mechanism**
  Erik Jan Marinissen (IMEC, Belgium)
- **IEEE Std P1838's Die Wrapper Register**
  Teresa McLaurin (ARM, USA)
- **IEEE Std P1838's Flexible Parallel Port**
  Hailong Jiao (Eindhoven University of Technology, The Netherlands)

12:30-14:00 Lunch

14:00-15:45 Session 8

14:00-15:30 8A: Special Session: IoT: Source of Test Challenges (plenary)

Organizer: Erik Jan Marinissen (IMEC, Belgium)

Moderator: Phil Nigh (GlobalFoundries, USA)

The semiconductor industry has been driving a major part of its growth through first the PC and more recently the mobile market. Unfortunately, the PC market is in decline and also the end of the growth curve for mobile products is in sight now that virtually everyone on the planet has a smartphone and/or tablet. Hence, the semiconductor industry is putting its bets on 'Internet of Things' (IoT) as the next application wave that will allow them to sell a lot of silicon real estate. Although what exactly IoT encompasses is under definition and hence still volatile, the first emerging products depict an image which is quite different from the traditional microprocessors or smartphone SOCs: small but with ubiquitous presence, wirelessly connected, energy harvesting, equipped with smart sensors, secure, and low cost. All these aspects have a profound impact on the challenges, solutions, and associated trade-offs for testing IoT chips and provide rich grounds for research.

- **IoT Trends & Test Challenges**
  Yervant Zorian - Fellow and Chief Architect - Synopsys, USA
- **Test Challenges in IoT from Technology and Design Point of View**
  Mario Konijnenburg - System Architect - imec, the Netherlands
- **IoT Test Challenges from Low Power and Energy Harvesting Viewpoint**
  Chih-Tsun Huang - Vice Director of IC Design - National Tsing-Hua University, Taiwan
  Ping-Hsuan Hsieh - Assistant Professor - National Tsing-Hua University, Taiwan
- **Testing Challenges for IoT Smart Sensors**
  Peter Cockburn - Senior Product Manager Test Cell Innovation - Xcerra Corporation, UK
- **Testing of Random Numbers and PUFs: Roots of Trust for IoT**
  Jeroen Delvaux, Vladimir Rožic, Bohan Yang, Dave Singelée, Ingrid Verbauwhede - KU Leuven, Belgium
- **Route of Trust for IoT Manufacturing Test**
  Cedric Mayor - CTO - Presto Engineering, France
- **Achieving 100x Test Cost Reduction: a Dream or Reality?**
  Robert van Rijsinge, Cocoy Reyes – NXP Semiconductors, the Netherlands

- **Panel Discussion**
  All speakers

15:45-16:00 Closing Session