21st IEEE European Test Symposium

Mövenpick Hotel Amsterdam City Centre
Amsterdam, the Netherlands
May 23 – 27, 2016

www.ets16.nl

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Vendor Sessions – Call for Submissions

The IEEE European Test Symposium (ETS) is Europe's premier forum dedicated to presenting and discussing scientific results, emerging ideas, practical applications, hot topics, and new trends in the area of electronic-based circuit and system testing.

ETS 2016 (ETS'16) will take place at Mövenpick Hotel Amsterdam City Centre in Amsterdam, the Netherlands. It is organized by the Technical University of Delft, which co-sponsors the event jointly with the IEEE Council on Electronic Design Automation (CEDA).

ETS'16 is offering commercial vendors the opportunity to give technical presentations in a track parallel to the technical paper sessions. These presentations will be listed in the symposium program along with the technical sessions, and should be targeted to the ETS technical audience. The Vendor Sessions differ from other ETS presentations in that company names, logos, and product names may be mentioned explicitly. Typical content includes product descriptions, case studies, best practices, and user testimonials. Attendance at the sessions is open to all symposium attendees, and vendor representatives will be able to hand out literature at the session.

Presentation opportunities of 30-minute duration are available on a first-come first-served basis, but priority will be given to those companies that are also corporate supporters of ETS'16 – see below. Proposals for the Vendor Sessions should be technical or application focused, rather than overtly sales-and-marketing focused. Proposal selection is based on the technical content and relevance to ETS audience and topics; priority will be given to ETS corporate supporters.

The areas of interest of ETS'16 include (but are not limited to) the following topics:

- *Analog Test*
- *ATE Hardware and Software*
- *Automatic Test Generation*
- *Board Test and Diagnosis*
- *Boundary Scan Test*
- *Built-In Self Test (BIST)*
- *Current-Based Test*
- *Defect-Based Test*
- *Delay and Performance Test*
- *Dependability and Functional Safety*
- *Design for Test(ability) (DfT)*
- *Design for Manufacturing (DfM)*
- *Diagnosis and Silicon Debug*
- *Economics of Test*
- *Emerging Technologies*
- *Failure Analysis*
- *Fault Modelling and Simulation*
- *Fault Tolerance*
- *GPU Test*
- *High-Speed I/O Test*
- *Low-Power IC Test*
- *Memory Test and Repair*
- *MEMS Test*
- *Microprocessor Test*
- *Mixed-Signal Test*
- *Multi-/Many-Core Processor Test*
- *Nanotechnology Test*
- *On-Line Test*
- *Power Issues in Test*
- *Reconfigurable System Test*
- *Reliability*
- *RF Test*
- *Security and Trust Issues in Test*
- *Self-Repair*
- *Sensor Test*
- *Signal Integrity Test*
- *SiP, Stacked, 3D IC Test*
- *SoC Test*
- *Soft Errors*
- *Standards in Test*
- *System Test*
- *Test Compression*
- *Test Quality*
- *Test Synthesis*
- *Thermal Issues in Test*
- *Validation and Verification*
- *Variability Issues in Test*
- *Yield Analysis and Enhancement*

Submissions

A submission to the ETS'16 Vendor Sessions can be an abstract, extended abstract, or full paper (max. six pages); submission of a full paper is preferred, but not required. Proposals should be submitted via the ETS'16 website; detailed submissions instructions can also be found there (go to http://www.ets16.nl, and then select Vendor sessions at the left menu). Key dates for submissions are:

- Submission deadline: **January 30**, 2016
- Notification of acceptance: **February 12, 2016**
- Camera-ready manuscript: **March 13, 2016**

More Information

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Visit the ETS'16 web page at: **http://www.ets16.nl**.