

# A System Level Boundary Scan Controller Board for VME Applications

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## Abstract

*This work is the result of a collaboration between INESC and LIP in the CMS experiment being conducted at CERN. The collaboration addresses the application of boundary scan test at system level namely the development of a VME boundary scan controller (BSC) board prototype and the corresponding software. This prototype uses the MTM bus existing in the VME64x backplane to apply the 1149.1 test vectors to a system composed of nineteen boards, called here units under test (UUTs).*

*A top-down approach is used to describe our work. The paper begins with some insights about the experiment being conducted at CERN, proceed with system level considerations concerning our work and with some details about the BSC board. The results obtained so far and the proposed work is reviewed in the end of this contribution.*

## 1. Introduction

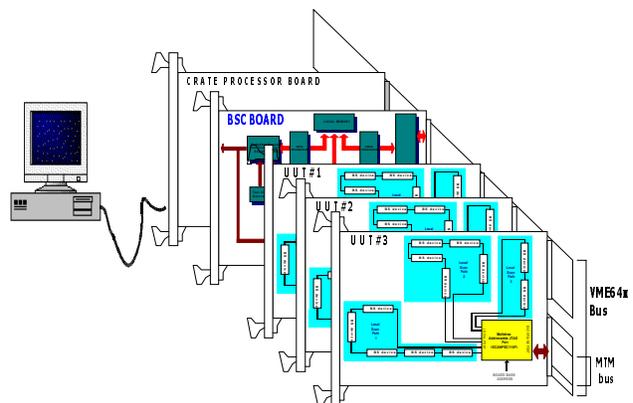
The Large Hadron Collider (LHC) being developed at CERN will be used as a common infrastructure for a number of experiments namely the Compact Muon Solenoid (CMS) experiment [1, 2]. One of the most complex systems of the experiment apparatus is the calorimeter trigger which is a high performance electronics and computing system able to process the huge amount of data produced by the detector. Ultimately the system will provide evidence of several physical particles including the Higgs boson.

The Upper Level Readout and Trigger (ULRT) interfaces with the detector channels and contains the electronic units to process the data. These electronic units are housed on 64 VME 9U crates, each containing one

CPU (crate processor board), one Data Concentrator Card (DCC) and 17 ULRT units [3].

Each crate uses a VME backplane (VME64x) to interface the processor board (the master board) with each system board. The crates will be placed in a cavern 100 m underground, close to the CMS detector, inaccessible during the operation of the LHC accelerator.

Given the complexity and organisation of the system it is mandatory to consider Design for Testability (DFT) and remote reconfiguration techniques in order to create a testable system not only during actual operation but also at other phases of the system lifetime [4]. An implementation of boundary scan testing at system level was proposed, that includes the boundary scan implementation at each board and the development of dedicated board - the boundary scan controller (BSC) board - to control the execution of the tests when the system is idle - figure 1.



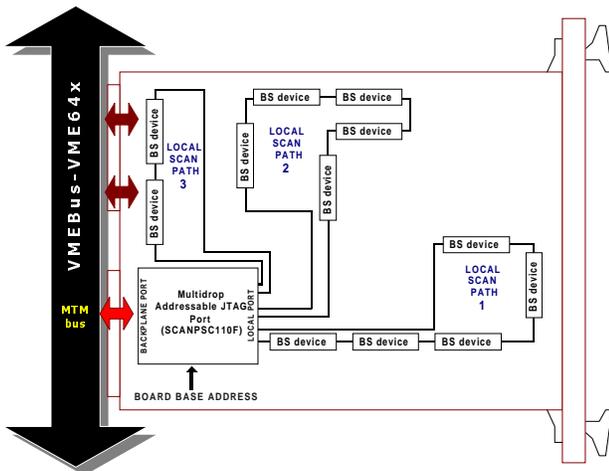
**Fig. 1** - Proposed system level boundary scan architecture.

## 2. Boundary Scan Test Architecture at Board Level

The test of a large system composed of several boards placed in a common backplane, such as the one considered here, poses several difficulties to the 1149.1 test standard [5]. The 1149.1 standard was oriented for testing a single board using a serial linked TDI/TDO scan path. This solution couldn't be implemented using a backplane bus where all test signals run in parallel in the bus.

The IEEE 1149.5 - Module Test and Maintenance Bus standard was considered for supporting the required test architecture [6]. This standard offers a solution to the integration of testable boards and/or modules into a testable and maintainable subsystem. The standard requires the use of specific interfacing devices (MTM-Bus Master and MTM-Bus Slaves) communicating through a backplane, using a structured protocol, not compatible with the 1149.1 standard. These devices are not yet available commercially. The boundary scan software test systems currently available use the 1149.1 protocol to communicate with the hierarchical devices placed in the backplane which make them unsuitable for use with 1149.5 devices.

Therefore a solution was presented using commercial available circuits called Boundary Scan Interface Devices. These devices provide a connection link between one or several scan chains in each board and the common test bus, thus forming a hierarchical test system - figure 2.



**Fig. 2** - The Multidrop Addressable JTAG Port from National Semiconductor is used as an interface device between the local scan paths and the MTM bus.

There are two of these devices commercially available, supported by boundary scan software: the

SCANPSC110F from National Semiconductor and the ABT8996 from Texas Instruments. The SCANPSC110F was chosen in our implementation [7]. This circuit provides the interface between three local scan paths and the backplane test signals [8]. The SCANPSC110F uses an addressable test access controller which eliminates the drawbacks of traditional methods (daisy chaining the boards TDI and TDO signals) while also providing the capability of partitioning one single board level scan chain into smaller chains (called local scan ports). These scan ports are independently connected to the system test bus, or all together forming a single local scan chain. This flexible configuration allows easier generation of test vectors by the ATPG.

This architecture extends the functionality of the IEEE 1149.1 Standard by offering an addressing scheme, which allows the test controller to communicate with a specific SCANPSC110F within a network of these IC's.

Each SCANPSC110F in one network is configured statically with a unique address (the configuration is hardwired) specified by the slot inputs, which can be the board base address. After being addressed using 1149.1 compatible protocol, the SCANPSC110F becomes the only device selected to receive additional 1149.1 test instructions.

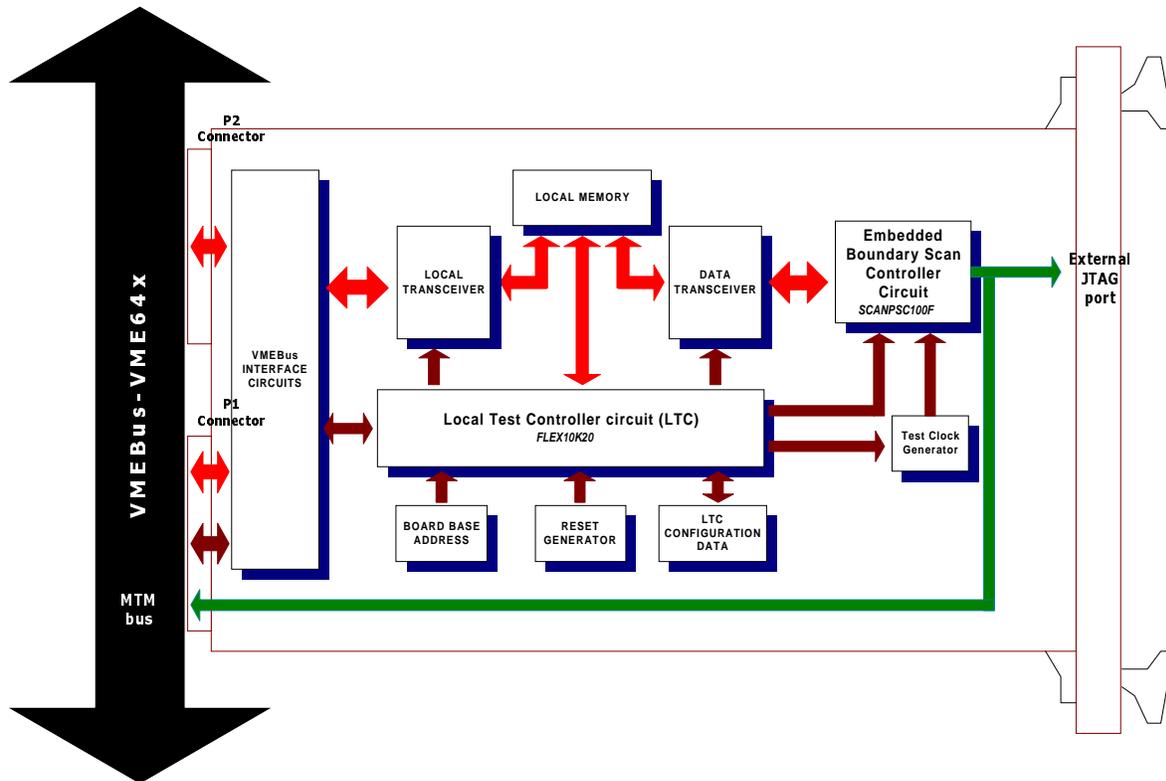
### 2.1. The MTM bus

The recent VME standard, called VME64 Extensions or VME64x adopts new P1/J1, P2/J2 connections with 160 pins, that include the IEEE Standard 1149.5 Module Test and Maintenance bus [9]. This bus is composed of five pins, MCLK, MCTL, MMD, MPR and MSD, used in our system as standard 1149.1 pins, with TDI and TDO running in parallel.

### 2.2. Backplane Testing

Testing backplane interconnections is also being considered during the tests of the prototype board. This type of test is the only one specific to the system. The backplane tests attempt to detect errors occurring during the backplane assembly process. Board pins may be bent, short or broken, boards can be misplugged and even backplane traces can be short or broken.

Testing the backplane is similar to testing a single board with the exception that, the components may be in different local scan paths and in different SCANPSC110F devices. For testing the backplane connections it is advisable to use boundary scan devices interfacing the VME connectors and to place them in the same local scan path - as it is exemplified in figure 2, with the local scan path 3. This type of testing is performed using a special address to select all the SCANPSC110Fs in the backplane.



**Fig. 3 - Boundary Scan Controller board.**

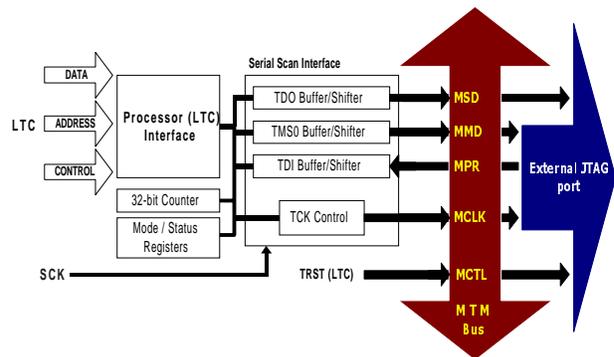
For testing the backplane additional information needs to be gathered [10]:

- *The backplane netlist* describing the interconnections between the boundary scan (BS) circuits interfacing the bus. This information needs to be updated each time a new configuration of the system is used (i.e. the number of boards connected).
- *The hierarchy of boundary scan devices* specifying the structure of the scan link at board level and at backplane level. It includes the information concerning the SCANPSC110F devices (device address, local scan ports) and the BS devices interfacing the backplane slots.

### 3. The Boundary Scan Controller Board

The Boundary Scan Controller board (BSC board) was implemented using a 6U VME board to be placed in the VME64 Extended bus (VME64x). The bus interface connectors used, P1 and P2, contain 160 pins distributed in five rows, z, a, b, c and d. The exterior rows (z and d) were used essentially to access the MTM bus signals which are not defined for the VME64. A simplified block diagram of the BSC board is shown in figure 3.

The SCANPSC100F, Embedded Boundary Scan Controller, generates the 1149.1 test signals applied to the MTM bus, or to the external JTAG port, figure 4.



**Fig. 4 - Block diagram of the SCANPSC100F and the connections to the MTM bus and to the external JTAG port.**

The BSC board introduces a small overhead in the VME operation, which means that the boundary scan tests can be conducted with little interaction with the VME processor board. This feature requires the use of large memories to store the test patterns and the corresponding

test results. The optimum amount of memory needed to implement this stand alone test procedure is one of the factors being evaluated by the planned tests of the prototype board.

The functionality of the BSC board is also independent of the VME protocol. This characteristic enables to re-use this board if another backplane is chosen.

The functionality of the main blocks of the BSC board will be analysed in the next sections.

### 3.1. Embedded Boundary Scan Controller Circuit - SCANPSC100F

This device operates by serializing and shifting the data received from the processor interface through the MTM bus - figure 4. The chip includes a buffer/shifter for TDI, TDO and TMS which is continuously updated during the test. A 32 bit counter is loaded with the number of test clock cycles to complete a scan operation or to run a Build-In Self Test (BIST). The circuit supports test clock frequency range up to 25 MHz.

### 3.2. VMEbus Interface Circuits

The integrated circuits CY7C960 Slave VMEbus Interface Controller and CY7C964 VMEbus Interface Logic were used to interface with the VME backplane. These circuits implement the transactions required by the VME bus protocol when accessing the BSC board. The VME bus is used to:

- Verify the current state of the board.
- Load the test vectors and the test control data to the local memory.
- Start, restart and stop the test.
- Read from the local memory the test results obtained from the UUT.

### 3.3. Test Clock Generator

The test clock signal is generated locally, in a frequency range between 391 KHz and 100 MHz, by a programmable clock generator. During boundary scan testing the upper limit of the test clock frequency will be determined by:

- The lowest maximum frequency supported by the boundary scan devices in the chain.
- The maximum allowed frequency for the embedded boundary scan controller (25 MHz) and backplane.
- Propagation delays, occurring in test signal paths.

The Local Test Controller (LTC) circuit programs the clock generator at the beginning of each test.

### 3.4. Local Test Controller (LTC)

The LTC is responsible for controlling the functionality of the test board. It was implemented in a Altera FLEX10K20 programmable logic device using the MAX+PLUS II development software. This PLD has some features adequate to the development process:

- The configuration of the device can be re-programmed on-line during the prototype development phase using a download cable or EPROM device.
- The amount of logic gates available (about 20,000) allowed the implementation of the required logic functions within one single device thus saving space and easing the simulation.
- The MAX+PLUS II, software development tool, was used to entry the design files (using AHDL and schematic files), to verify and simulate the design and to download the resulting configuration data to the device.

The Local Test Controller functions can be divided in five sub-modules or blocks briefly described next.

*Test Control State Machine* - State machine that controls the execution of the test and the state of the board. After reset, the machine waits for a START\_TEST instruction written in the corresponding register by the VME processor, to start the test. After the completion of the test a Status Register is assigned with ENDED status.

*VME Configuration* - Block responsible for configuring the operation mode of the VME Slave bus interface circuits, namely the configuration of the board address. The BSC board has a programmable address that is loaded into the VME slave at power on.

*Data Transfer Controller* - This block manages the data transfer between the local memory, the embedded boundary-scan controller and the LTC itself.

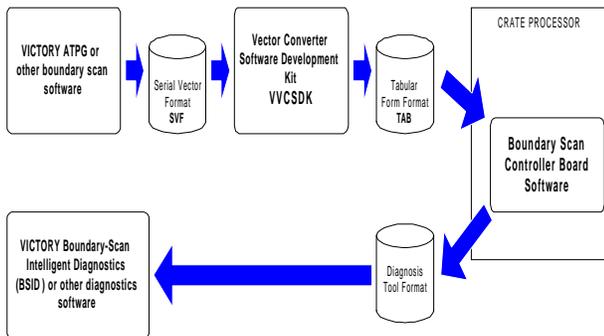
*Status/Instruction Registers* - The LTC contains two registers accessed by the VME processor board. The Instruction Register is loaded mainly with the instructions to start and to stop the test. The Status Register contains the current state of the test, which is updated by the LTC.

*Clock Programmer Machine* - This module is used to program the Test Clock Generator through a serial bit chain. The test clock frequency is set up by shifting into a set of registers the configuration bit pattern synchronously with a low frequency clock signal.

## 4. Boundary Scan Test Development Tools

The BSC board is currently being tested using Teradyne's VICTORY boundary scan test software [11].

This software package allows the generation of boundary scan tests in Serial Vector Format (SVF) using an ATPG. This format developed jointly by Teradyne and Texas Instruments provides the mean of exchanging boundary scan test vectors between the ATPG and the ATE. This format is transformed into an intermediate tabular format or truth table format using the Vector Converter Software Development Kit (VVCSDK 1.10) provided by VICTORY. The truth table format represents the logic levels of each 1149.1 test signal. In figure 5 it is shown the complete data flow corresponding to the development of the test vectors its application and the diagnostic of the test results.



**Fig. 5** - Data flow from test generation to test result analysis.

When the test of one or all the boards in the crate is required, the crate processor runs the test software package that loads the appropriate data stimuli in the BSC board and waits until the test is completed. The BSC board will indicate the end of the test by writing the STATUS register. Further diagnostics about a given failure can be derived by transferring the contents of the memories of the BSC board having the test results to a file. The same test software package provides the way to perform this transference of test results.

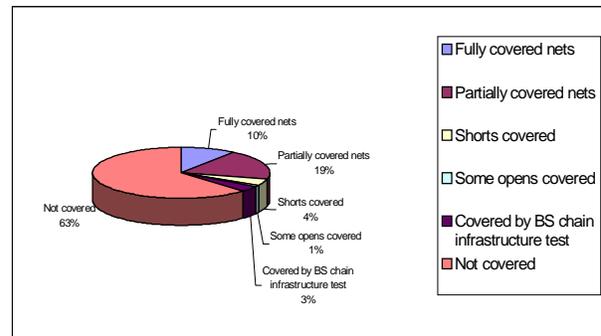
## 5. Testing the BSC Board Using Boundary Scan

The BSC board itself includes boundary scan test facilities used to partially test the board. The LTC circuit and the transceivers include boundary scan cells in most of their pins, which are connected through their JTAG test access ports, forming a single boundary scan chain accessible through a dedicated connector. The boundary scan tests developed include:

- BS chain infrastructure test: this test verifies the chain formed by the BS circuits and the correctness of the

devices according to the board netlist, by testing the identification register when available.

- Board interconnections test: a limited number of interconnections is tested using the virtual access points provided by the boundary scan cells. This test covers the connections involving only these cells, and the nets placed at a constant voltage level observed by a boundary scan cell. The figure 6 shows the test coverage of the interconnection and infrastructure test. In fact, 37 % of the nets are somehow tested using this type of test, although only about 10 % are fully covered. The low coverage is due mainly to the large number of nets involving the VME interface circuits and the VME connectors, which don't have boundary scan implementation.
- Cluster test: some blocks of logic, designated by logic clusters, namely the memory circuits, and the board base address, are tested with a functional test using the virtual access provided by the boundary scan cells. These pins are used to control the state of the memory devices (read/write) and to provide the data and the address.



**Fig. 6** - BSC board test coverage for interconnections and infrastructure test.

Some of the circuits without a boundary scan implementation are tested using a functional test.

Although the testing capabilities of boundary scan are widespread, its use as a board debugging is also very valuable. During the board development the VME interface was not working, leaving the local part of the board inaccessible using VME operations. A simplified version of the PLD configuration with the main functions was downloaded to the device. The BS bus interface provided the access to the memory circuits allowing to load the test vectors and the control data preceding the start of the test and to read back the test results after the test has been concluded. Using the boundary scan access it was possible partially test the local functionality of the board, leaving the VME interface part test for a functional test.

## 6. Conclusions and Future Work

The board has been delivered in the beginning of this year. Preliminary tests have been made using boundary scan test, which presents a fault coverage of 37 % only for the interconnections. These tests permitted to locate a few assembly problems and to fully test the Altera IC interconnections. The test coverage was increased with the cluster tests used to test the memories, the embedded BSC circuit, the board base address and the test clock generator.

Using boundary scan to access the local memories and the embedded boundary scan controller circuit (SCANPSC100F) allowed to partially test the local part of the board.

A simplified version of the BSC board software is being used to download a simple test file into the BSC board memory. This procedure will accelerate the debug of the board and will permit to know the optimal amount of memory required to run stand alone tests. There isn't a definitive decision about the boundary scan software to be used for generating the tests and for diagnosing the results, although the use of SVF as an intermediate format seems to be certain.

To increase fault coverage, at board and system level, and due to the unavailability of boundary scan cells in the VME interface circuits, it is mandatory the use of boundary scan transceivers to interface the VME connectors at each board. The objective of this modification would be for testing purposes. However, this could be unacceptable given the limited area and power available for each board.

Another possibility under evaluation is to connect the unused PLD pins, in order to use them as additional tester pins thus increasing the fault coverage of the board without additional cost.

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