# Testable Interconnects for a Board Self-Test Approach

Ulf Pillkahn , Siemens AG   Munich
ulf.pillkahn@icn.siemens.de

## Abstract

In this paper, a novel technique is presented for the verification of board level connections on PCBs. The time domain method is used to identify whether a pin connection is faulty or not. The test pulse - and evaluation circuitry is part of the chip. Although the chip size increases slightly, the method is highly efficient. No Automatic Test Equipment (ATE) is necessary to carry out the test and since only the physical behaviour of the connection from the internal driver via pin to board is examined, no test vectors are needed. The test time and the test preparation time are lower compared with conventional test methods.

## 1 Introduction

At the chip level, fabrication and packaging technologies are creating increasingly dense integrated circuits. In addition, emerging technologies and assembly processes for electronic circuit cards are producing boards with greater solder joint densities. Increasing density will eventually make traditional mechanical accessibility unachievable, requiring new test strategies.

A number of methods have been implemented to provide a means of detecting structural failures. These methods range from functional board testers (FBT) to In-circuit testers (ICT) and combinational testers (ICT and FBT).

Boundary Scan was created to provide an improved technique for screening structural faults through reduced test programming time and improved fault coverage [Ba92]. Boundary Scan uses scan registers (Boundary Scan cell) to enhance the controllability and observability ( Figure 1). The storage cells in the register are used as observation points and/or control points.

Testing interconnects and/or logic external to chips the External Test Mode is applied [St95]. A test pattern is loaded into scan register A of IC 1( Figure 1). Chip one carries out an Update operation, where the data drives from the register to the output pad. Chip two carry out a capture operation, where the data on its input pad are loaded into register B. To compare the data from register A and the response in register B the data in the scan path must be shifted out. For a Self Test of the board is the Boundary Scan approach not applicable:

- the effort to compute or store the test pattern on board is usually beyond the board performance.
- The comparison of the actual and expected test vectors is to complex and to time consuming for microprocessor boards in telecommunication.

The paper presents a proposal for the test of board level connections independent from external test equipment. The chip itself detects the error and communicates with the board test controller, literally saying “This is what is wrong with me” (Figure 2).

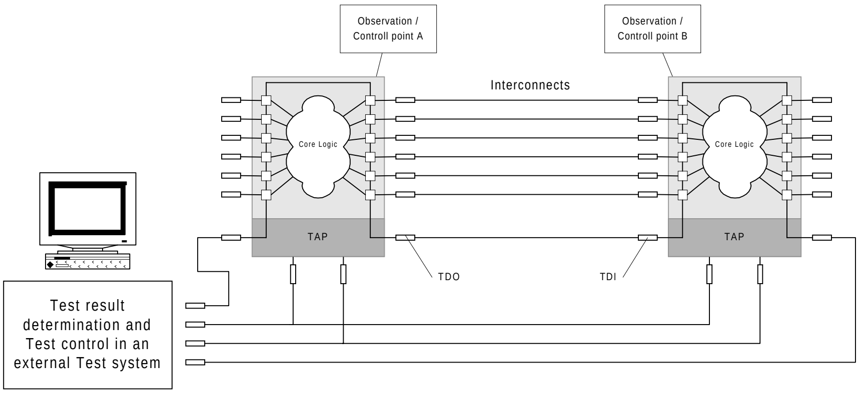


**Figure 1 Boundary Scan uses “silicon nails” to observe I/Os. The test is controlled from an external test device**

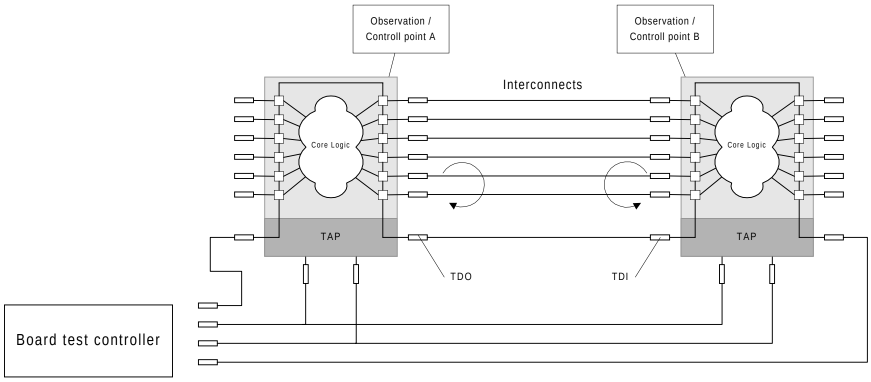


**Figure 2 Instead of shifting out the data in the scan path to see (extern) if the correct response was received, the test result can immediately obtained from the response on observation point A.**

The test result can be assessed within the IC since no communication between observation point A and B, like in the Boundary Scan Extest, is required. The advantage of this technology is that this test method gives the board the intelligence to do a power-on self- test, diagnosis and repair. Remote verification of the diagnosis as well as repair can then take place. This is important for accessing telecommunication equipment buried in remote locations.

## 2 Test Principle

The test aims to verify that the connection from the control logic to the pad is correct (Figure 3). As described earlier only one observation point is used in this approach.

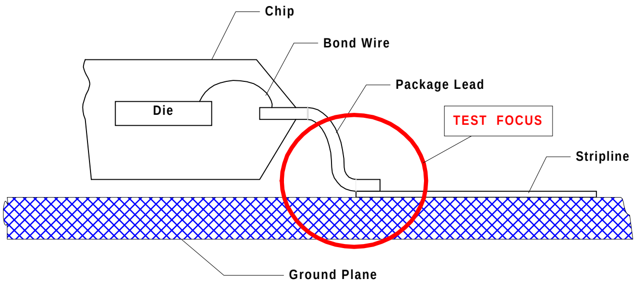


**Figure 3 Cross Section Model of the Connection Chip – Board**

This can only be achieved by considering the connection as a transmission line and examine the response from a test pulse.

As speeds increase, line inductance begins to cause overshoot and ringing in short lines and effects of wave propagation such as delay and reflection, in long lines. A lot of publications deal with the problem of interconnections on board and chip level. Most of them focus on optimizing the design for high-speed purposes. Propagation delay, parasitic pin capacitance and inductance and design parameters for packages and methods for modeling the behaviour are of concern [Li98, Te93, HP98]. Although the situation is similar, the problem is now faced from the other side. The connection has to be stimulated such that the response can be evaluated and assessed from an internal point in terms of open, short or a valid connection.

### 2.1 The Time Domain Reflectrometry Principle

A common method for evaluating a transmission line is the time domain reflectometry (TDR) [HP98].

When a high-speed electrical signal travels through a transmission line, a propagating electromagnetic wave will move down the line. If the edge transition time of the signal is less than the time it takes for the signal to travel from source to load and return from load to source the trace length becomes electrically “long” and should be treated as a transmission line (Figure 4).

This is because the signal reflects back to the source after the next edge-triggered event occurs. At any point in time, the total voltage becomes the sum of all the individual voltage sources present. Consequently, the information of the signal could be destroyed - the device may cease to function properly.

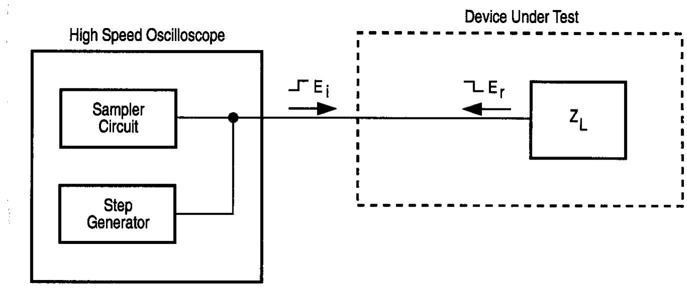


**Figure 4 The TDR principle**

## 2.2 Conditions for using TDR for interconnect test

A line can be regarded as electrically long, if the one way propagation delay from transmitter to receiver is equal to or shorter than the propagation time of the trace with round-trip reflection. Assuming a connection with 2.5 cm line length it says that with a rise time shorter than 250 ps the line should be modeled as transmission line. A line length greater than 2.5 cm or a rise time shorter than 250 ps could cause functionality concerns if the trace is improperly terminated. However, it should be noted, that transmission line analysis always gives the correct answer, irrespective of the rise time. If the trace is not terminated with a load resistance equal $Z_0$ of the trace, the energy that is not delivered to the load will be reflected [Ba90, Mo99]. Thus, for further examination the transmission line model (Figure 5) is used. Since the line resistance is negligible and attenuation is not of interest for inspecting the load resistance a lossless transmission line is assumed.

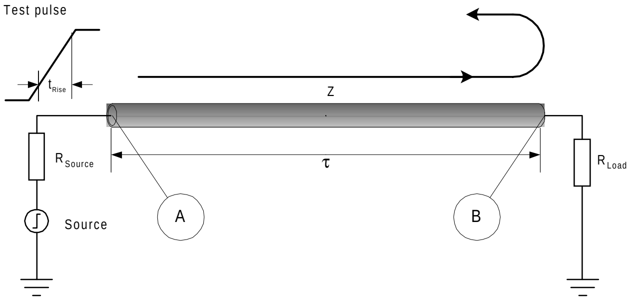


**Figure 5 Transmission Line Model**

## 2.3 Theoretical Analysis Techniques

Assuming the transmission line model the initial voltage step on the source end can be calculated using the resistive divider formed by the source resistance of the driver $R_{source}$ and the impedance $Z_0$.

$$V_A = \frac{Z_0}{R_{Source} + Z_0} \cdot V_S$$

and the reflected wave is

$$V_R = \frac{R_{Load} - Z_0}{Z_0 + R_{Load}} \cdot V_0$$

After 2τ the voltage on the source side is $V_A + V_R$. $R_{Load}$ can determined by measuring the magnitude on A:

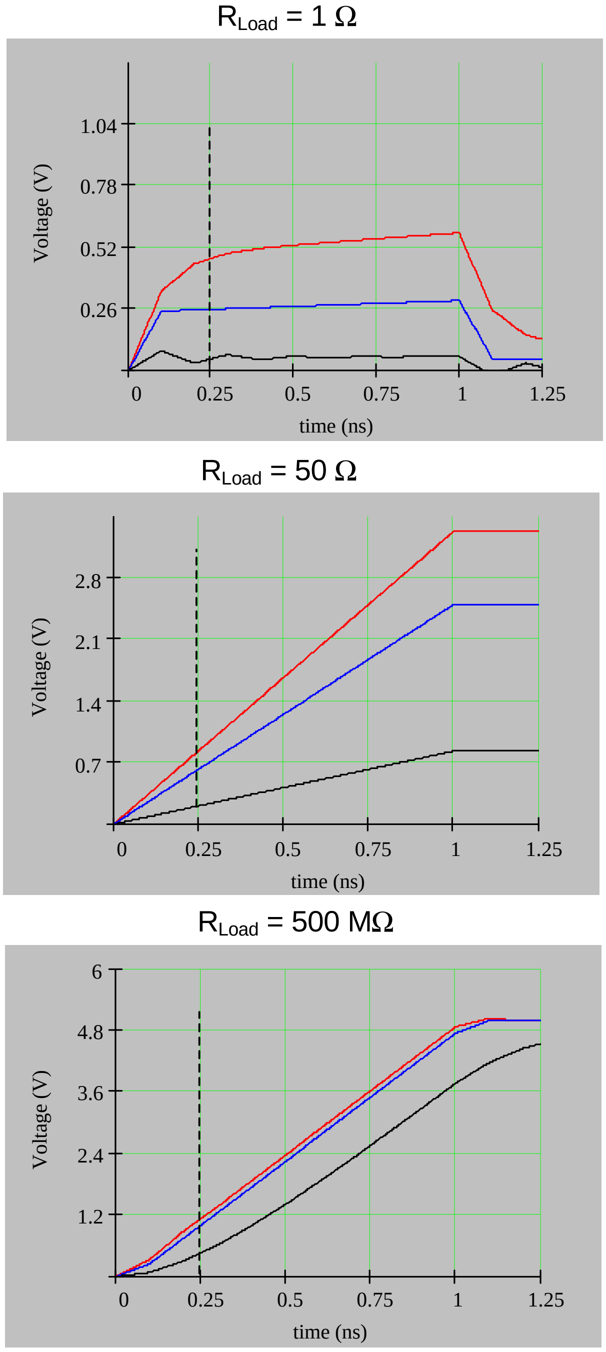
$$R_{Load} = Z_0 \cdot \frac{V_{2\tau} - V_A + V_0}{V_0 - V_{2\tau} - V_A}$$

Measuring the step response until 2τ guarantees that no other drivers on the same line influence the voltage on the load end. This would be a problem, if $R_{Load}$ would be calculated with the static end voltage and other drivers on the interconnect influence the voltage on the load side. Calculated waveforms with different combinations of $R_{Source}$ and $R_{Load}$ are shown in Figure 6 ($R_{source}$ =5Ω,50Ω and 250 Ω).

The Finite-Difference Time-Domain Method was used for the calculation [Ta95]. It can be seen that $R_{Source}$ must be taken into account for the evaluation of the response at t = 250ps.

## 2.4 Evaluation and Interpretation of the Test results

It is assumed that the impedance $Z_0$ is constant for all connections per chip. Thus one reference value per IC is necessary. The reference value is the calculated measured value for a good connection. $Z_0$ is the package specific impedance and can be determined [Mo96, Mo99, Go94] or is given from the manufacturer. Once the step response is measured, the value can be compared with the reference value. The diagram in Figure 8 shows how to interpret the test results to decide whether the connection is faulty or not.



$R_{Load} = 1\ \Omega$

$R_{Load} = 50\ \Omega$

$R_{Load} = 500\ M\Omega$

**Figure 6 $V_A$ for different combinations of $R_{Load}$ and $R_{Source}$**

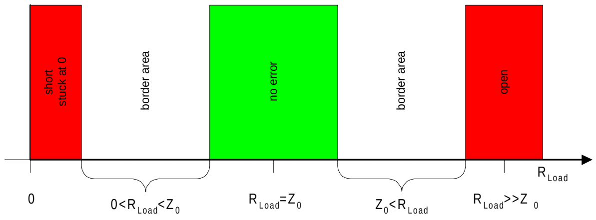


**Figure 7 Interpretation of the $R_{Load}$**

## 3 Experiments / Results

To verify the test method a test jig was developed (Figure 8). A pin from a PLCC package is connected via a gold bond wire and a coaxial cable to a pulse generator and stimulated with a ramp source voltage with a rise time of 500 ps.

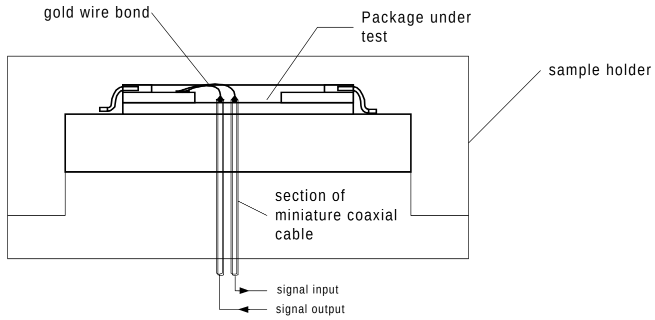


**Figure 8 cross section of the test fixture**

The step generator produces a positive-going incident wave that is applied to the transmission system under test. The step travels down the transmission line at the velocity of propagation of the line. If the load impedance is equal to the characteristic impedance of the line, no wave is reflected. If a mismatch exists at the load, part of the incident wave is reflected. The reflected voltage wave was obtained with the Time Domain Reflectometer (HP 54750A).

The calculated and measured voltages on A are presented in Figure 9. A smaller source resistance lead to a higher $V_A$ Magnitude from the referring load resistance. Differences between the calculated and the measured values are due to parasitics from the test jig.

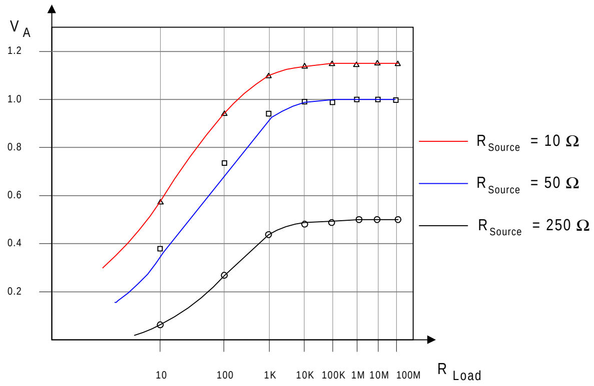


**Figure 9 Calculated and measured results for the magnitude on A**

## 4 Test Architecture

The Interconnect test is part of a hierarchical test concept. The chip detects whether all pin connections are as supposed (Figure 10) and communicate the result to the board test controller [Pi98]. The test information can be exchanged with a system test controller or a diagnose center.

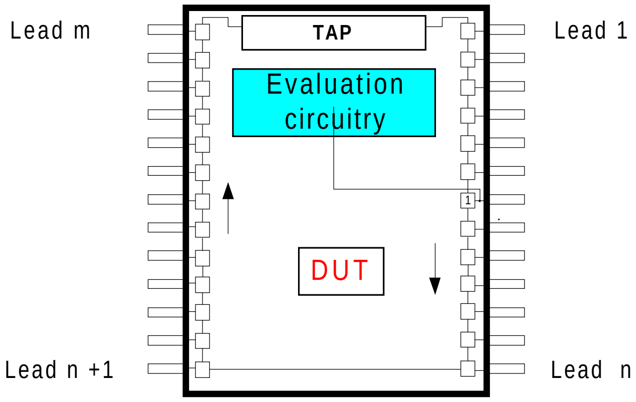


**Figure 10 Test control within the Chip – the pins are tested one by one**

Pulse generator: The pulse that is generated by the Boundary Scan output driver is sufficient in terms of rise time. (discussed in chapter 1)

Test response measure: The circuitry for the response evaluation is a trade-off between accuracy and chip overhead. Using an analog – digital converter (ADC) would be the maximum in terms of precision but the chip size is not acceptable [De91]. The present implementation uses a window comparator. A positive and negative tolerance value is added to the calculated reference value. The window comparator can determine whether or not the measured value lies between the two boundaries (no error) or outside (error).

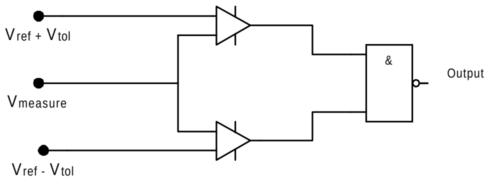


**Figure 11 Window comparator**

Board: The board test controller (BTC) initializes all testable chips and starts the test simultaneously for all chips (Figure 12). The BTC is the interface for other system parts and diagnosis tools.

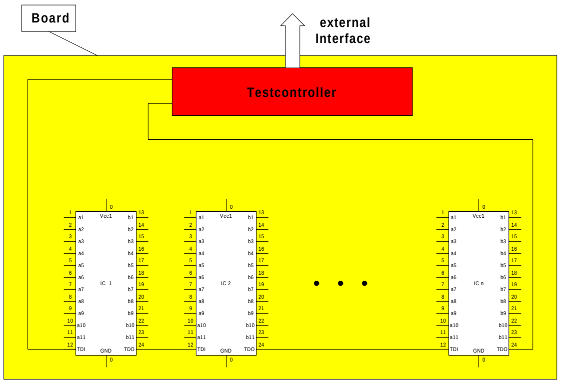


**Figure 13 Test control on Board**

## 5 Conclusions

A new technique to test solder connections from pin to board has been presented. Experiments attest the accuracy of the method compared with calculated data. The chip overhead is slightly higher than typical Boundary Scan circuits since all cells are designed as Input / Output cells and the logic for response verification is added.

Since this is a radically new technique for testing interconnects the trade-off between test coverage / test accuracy and test cost / chip space can be optimized. Further investigations aims to reduce the required chip space and to improve the evaluation circuit.

To transfer the technique in a general model this can be applied to different packages and chip families.

## 6 References

[Ba90] Bakoglu, H.B.:"Circuits, Interconnections, and Packaging for VLSI", Addison-Wesley Publishing Company, Menlo Park, California, U.S.A. 1990

[Ba92] Barker, K. P.: Boundary Scan Handbook. Boston, Mass.: Kluwer Publishing 1992

[Co88] Coombs,C.F. Jr.: "Printed Circuits Handbook", McGraw-Hill Book Company, San Francisco, California, U.S.A. 1988

[De91] Demler, M.J.: "High Speed Analog to Digital Conversion", Academic Press, Inc., San Diego, California, U.S.A 1991

[Ga87] Gardiol,F.E.: "Lossy Transmission Lines", Artech House, Inc.,Norwood, MA 1987

[Go94] Goel, A.K.: "High Speed VLSI Interconnections – Modeling, Analysis and Simulation", John Wiley & Sons, Inc., New York, U.S.A. 1994

[Gr98] Granzow, K.D.: "Digital Transmission Lines – Computer Modelling and Analysis", Oxford University Press, New York, U.S.A. 1998

[Ha88] Hart, B.L.: "Digital Signal Transmission – line circuit technology", Van Nostrand Reinhold (UK) Co. LTD, Berkshire, England 1988

[HP98] "Evaluating Microstrip with Time Domain Reflectometry" Application Note 1304-1, Hewlett - Packard Company 1998

[Li98] Li, T.:"Layout Extraction and Verification Methodology for CMOS I/O Circuits" DAC 35th Proceedings pp. 291-296, San Francisco 1998

[Mo96] Montrose, M.I.: "Printed Circuit Board Design Techniques for EMC Compliance", IEEE Press New York, U.S.A. 1996

[Mo99] Montrose, M.I.: "EMC and Printed Circuit Board – Design, Theory, and Layout Made Simple", IEEE Press New York, U.S.A. 1999

[Pi98] Pillkahn, U.: "Flexibel einsetzbares Teststeuermodul für digitale Baugruppen" 10. Workshop „Testmethoden und Zuverlässigkeit von Schaltungen und Systemen" Stuttgart 1998

[Po90] Pozar, D.M.: "Microwave Engineering", Addison Wesley Publishing Company Reading, Massachusetts, U.S.A. 1990

[Pr89] Prasad, R.P.: "Surface Mount Technology – Principles and Practice" Van Nostrand Reinhold New York, U.S.A. 1989

[St95] ANSI/IEEE Standard 1149.1b "IEEE Standard Test Access Port and Boundary Scan Architecture", IEEE Standards Board, 345 East 47th Street, New York, NY 10017 1995

[Ta95] Taflove, A.: "Computational Electrodynamics – The Finite-Difference Time-Domain Method", Artech House, Boston London 1995

[Te93] Tewksbury, S.K.: "Microelectronic System Interconnections – Performance and Modeling", IEEE Press New York, U.S.A. 1993