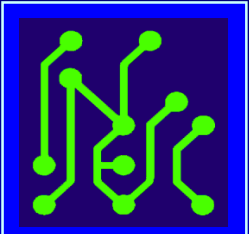

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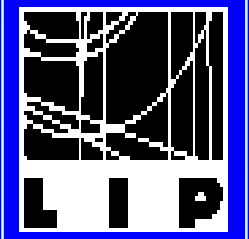

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A System Level Boundary Scan Controller Board for VME Applications

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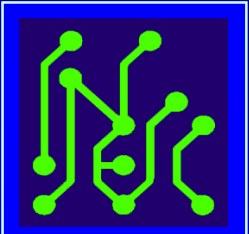

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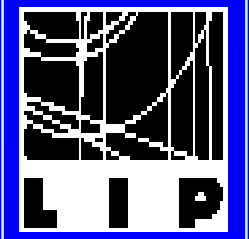

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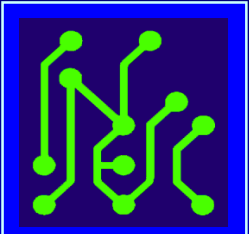
Outline of the Presentation

- Introduction.
- Boundary Scan Architecture at Board Level.
- The Boundary Scan Controller (BSC) Board.
- Boundary Scan Test Development Tools.
- Testing the BSC Board.
- Conclusions & Future Work.



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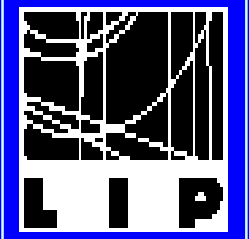

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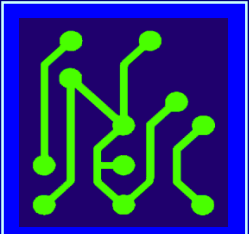
Introduction - I

- The CMS experiment under preparation at CERN has some challenging testing difficulties due to the organisation and inaccessibility of the electronic processing units (VME64x boards).

- To increase testability extensive boundary scan implementations are being used - at board level, and later at system level (in each crate).



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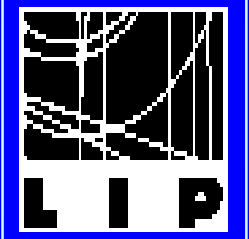

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Introduction - II

- Each crate in the Upper Level Regional Trigger (ULRT) system contains 19 electronic units or boards:
  - One processor board,
  - One Data Concentration Card board,
  - and 17 ULRT boards (UUTs).
- The Boundary Scan Controller (BSC) board will be used to execute boundary scan tests in each board of the crate.

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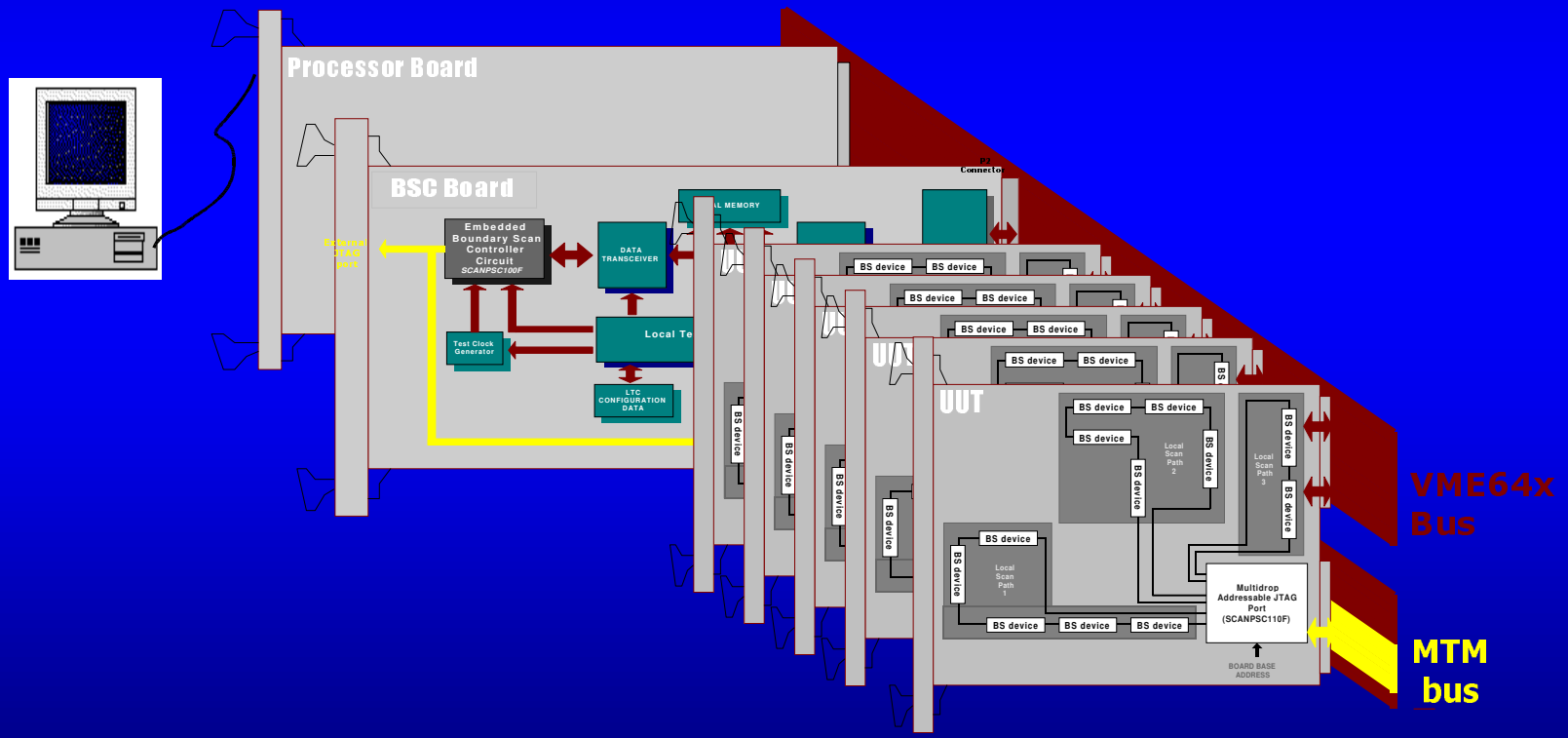
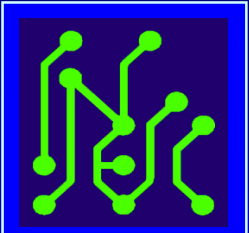
Introduction - III

Upper Level Regional Trigger (ULRT) system





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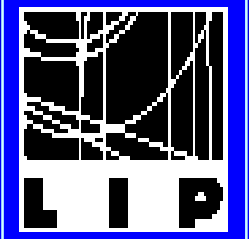

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Boundary Scan at Board Level - I

- The MTM bus in the VME64x backplane is used as a standard 1149.1 boundary scan path.
- The chain of BS devices in each board interfaces the MTM bus using a special device - BS Interface Device - that operates using the 1149.1 protocol.
- The MTM 1149.5 standard was considered for this implementation but rejected due to unavailability of support.

Boundary Scan at Board Level - II

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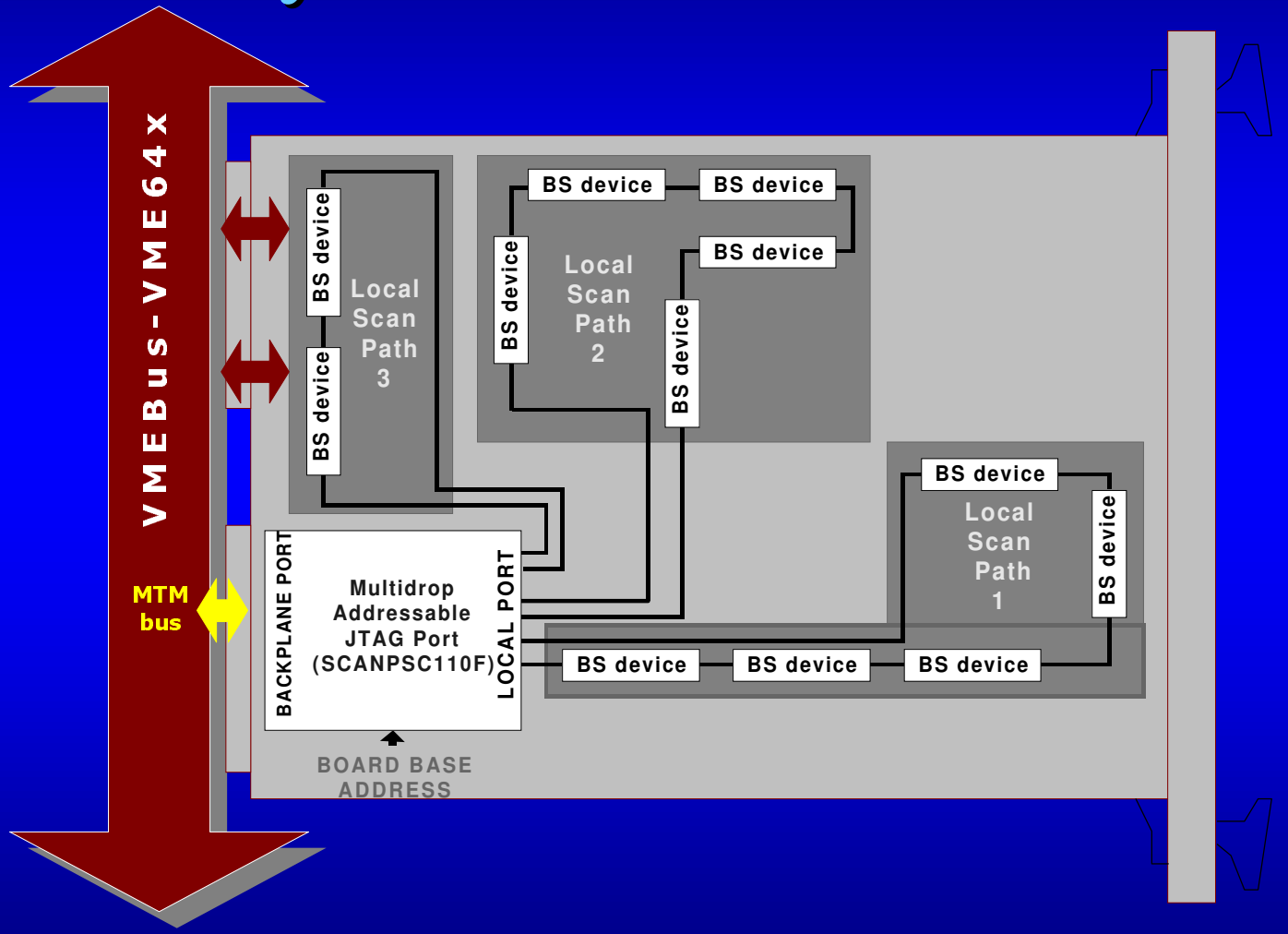

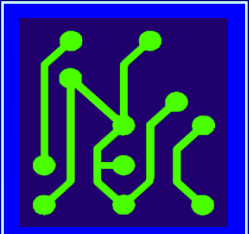

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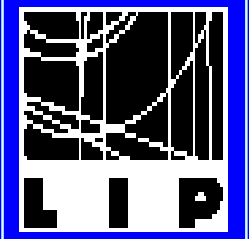

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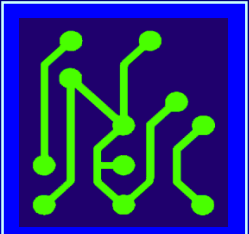
Boundary Scan at Board Level - III

- The BS Interface Device (SCANPSC110F) allows the partitioning of the board scan chain into three local scan chains - simplifies the test generation.
- Testing a single board is achieved by addressing one single BS Interface Device.
- Backplane interconnection test is also being considered.



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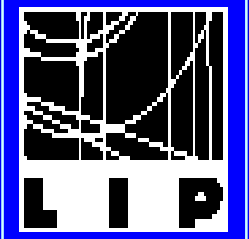

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The BSC Board - I

- The BSC board is responsible for the application of the test vectors using the MTM bus.
- The control of the test operations is performed by a programmable device (PLD). The use of fairly large memories allows the application of long tests.
- VME Interface devices are used to manage the VME communication protocol during the execution of test commands.

The BSC Board - II

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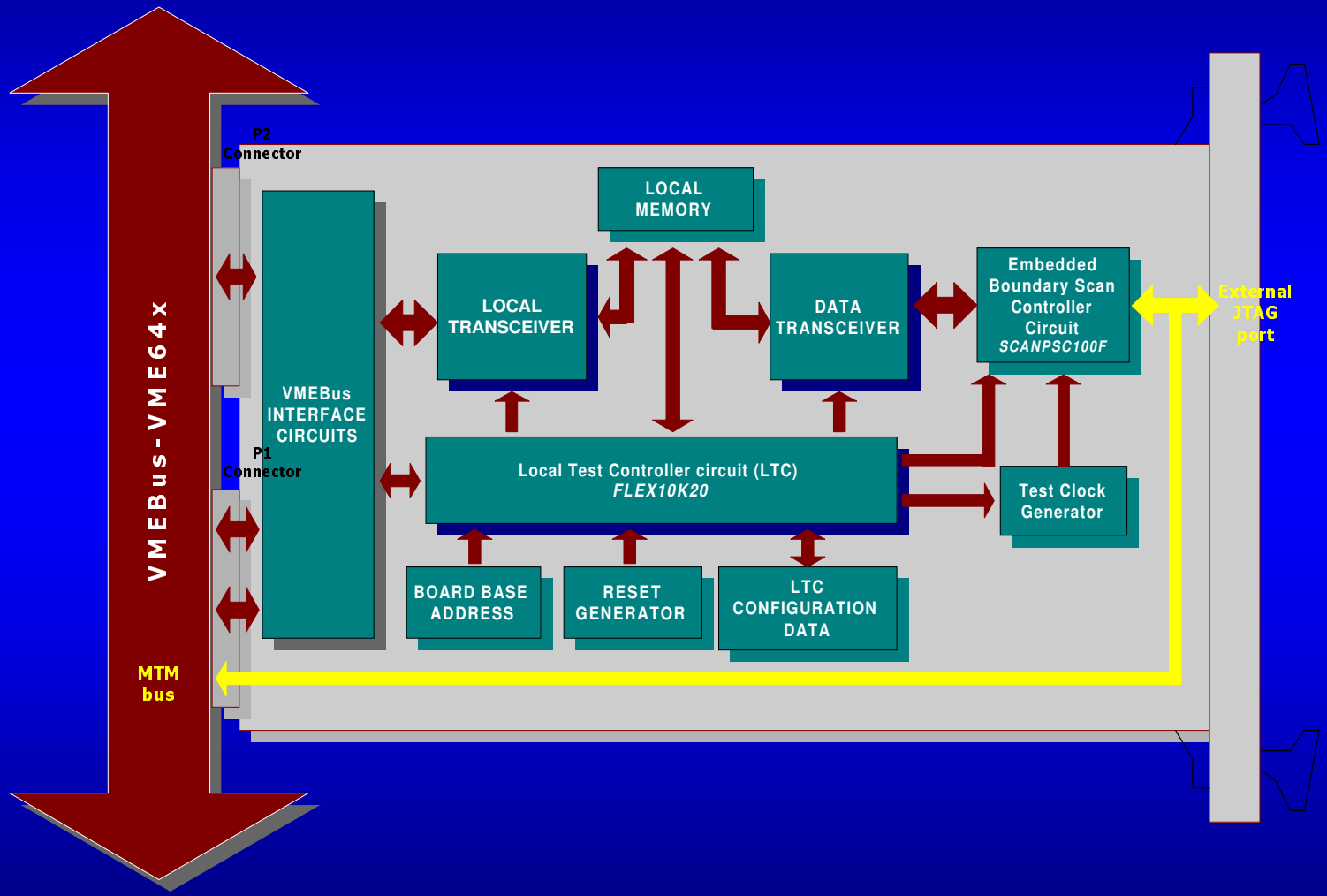

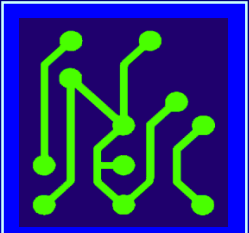

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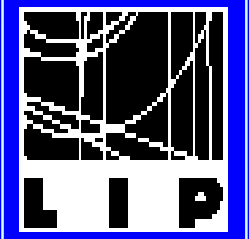

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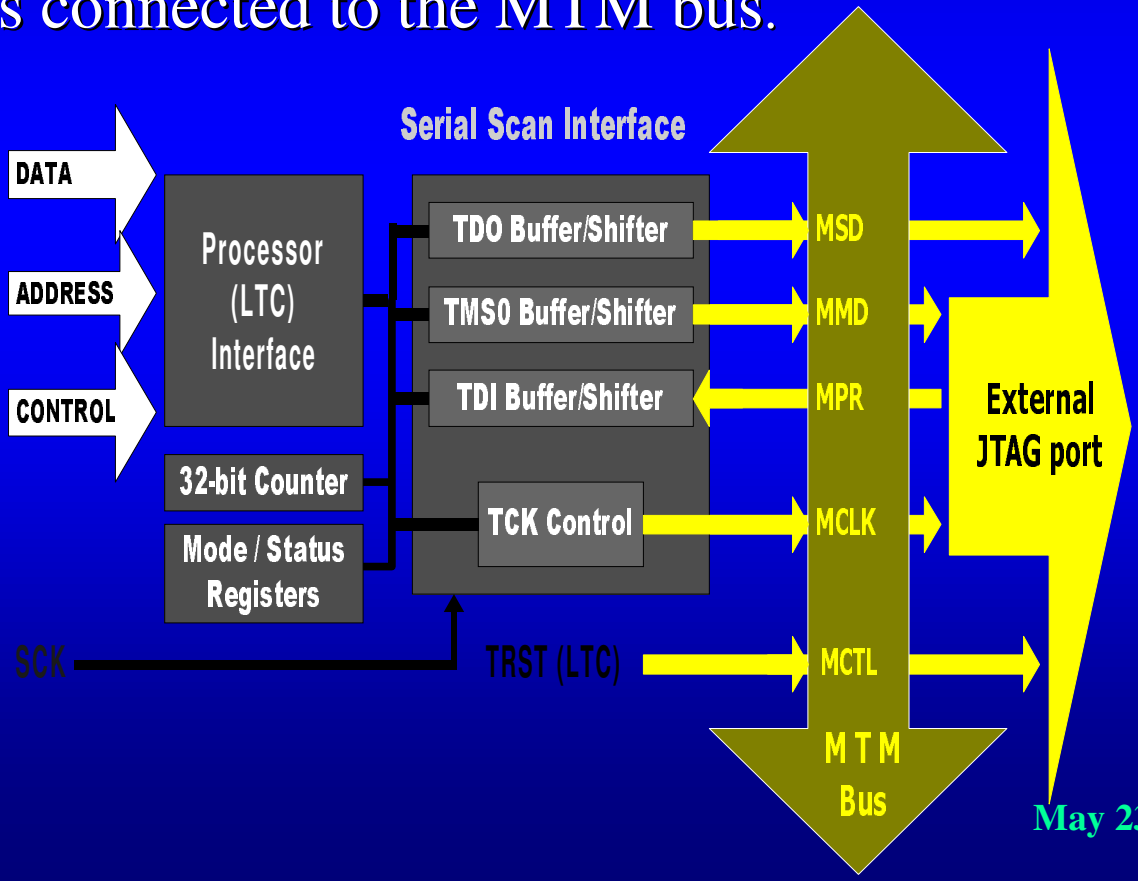
The BSC Board - III

- An Embedded Boundary Scan Controller (SCANPSC100F) controls the application of the test vectors using the 4 TAP signals connected to the MTM bus.



The BSC Board - IV

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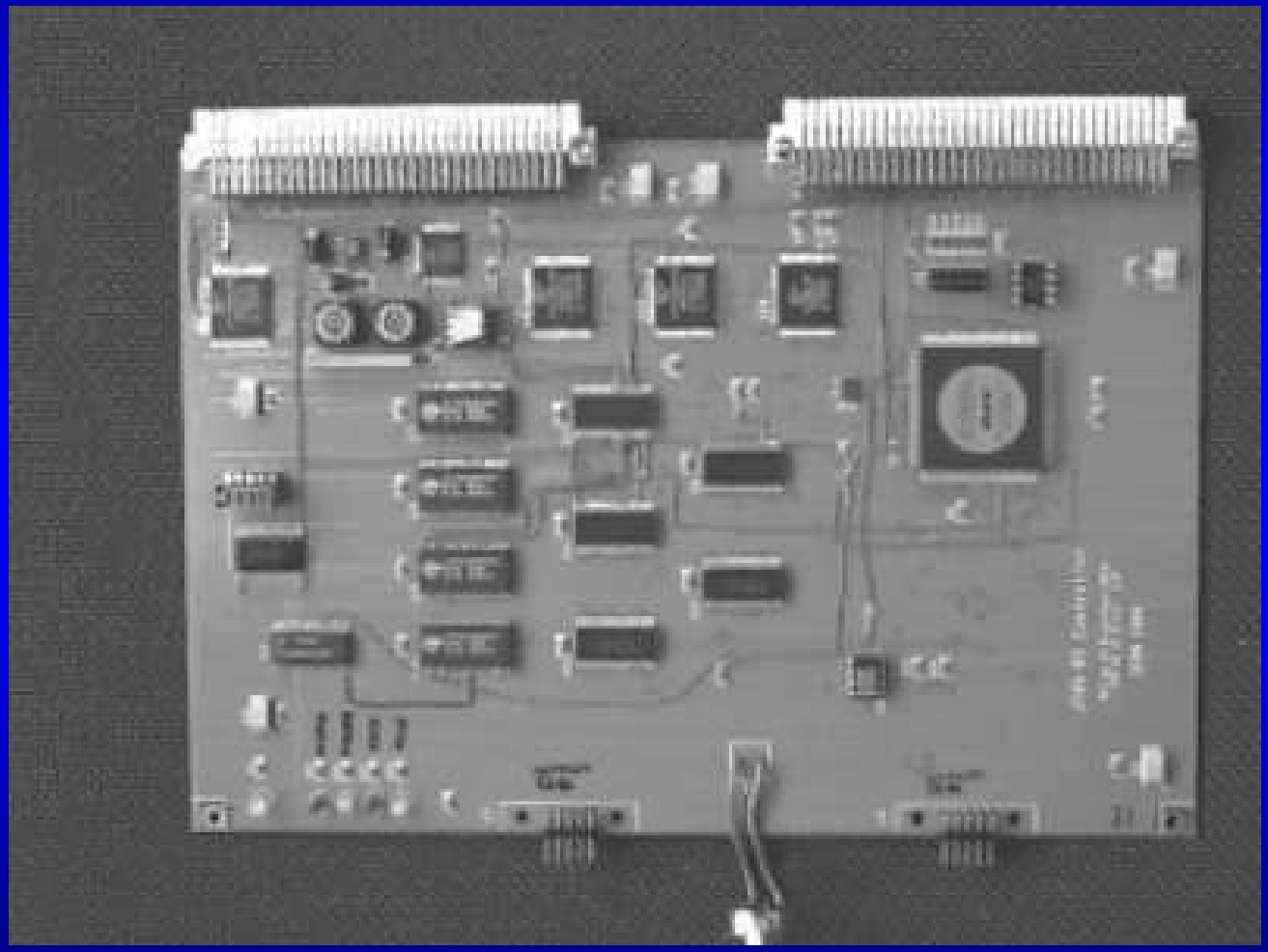

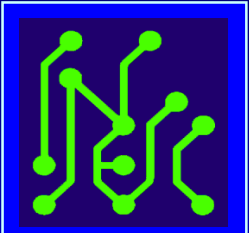

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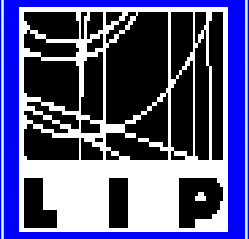

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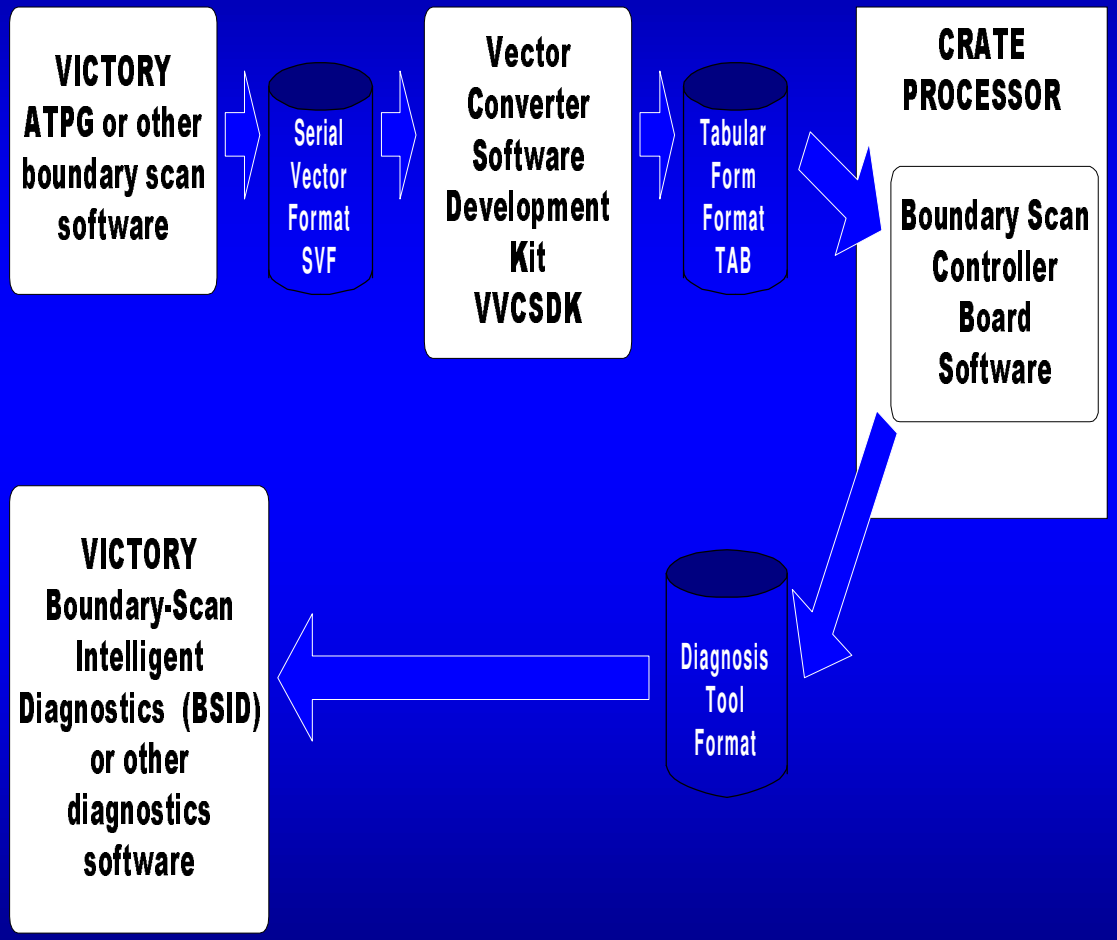
Boundary Scan Test Development Tools

- Test vectors are generated (in SVF format) using a commercial ATPG.
- Tests results are presented in a suitable format for the diagnosis tool.



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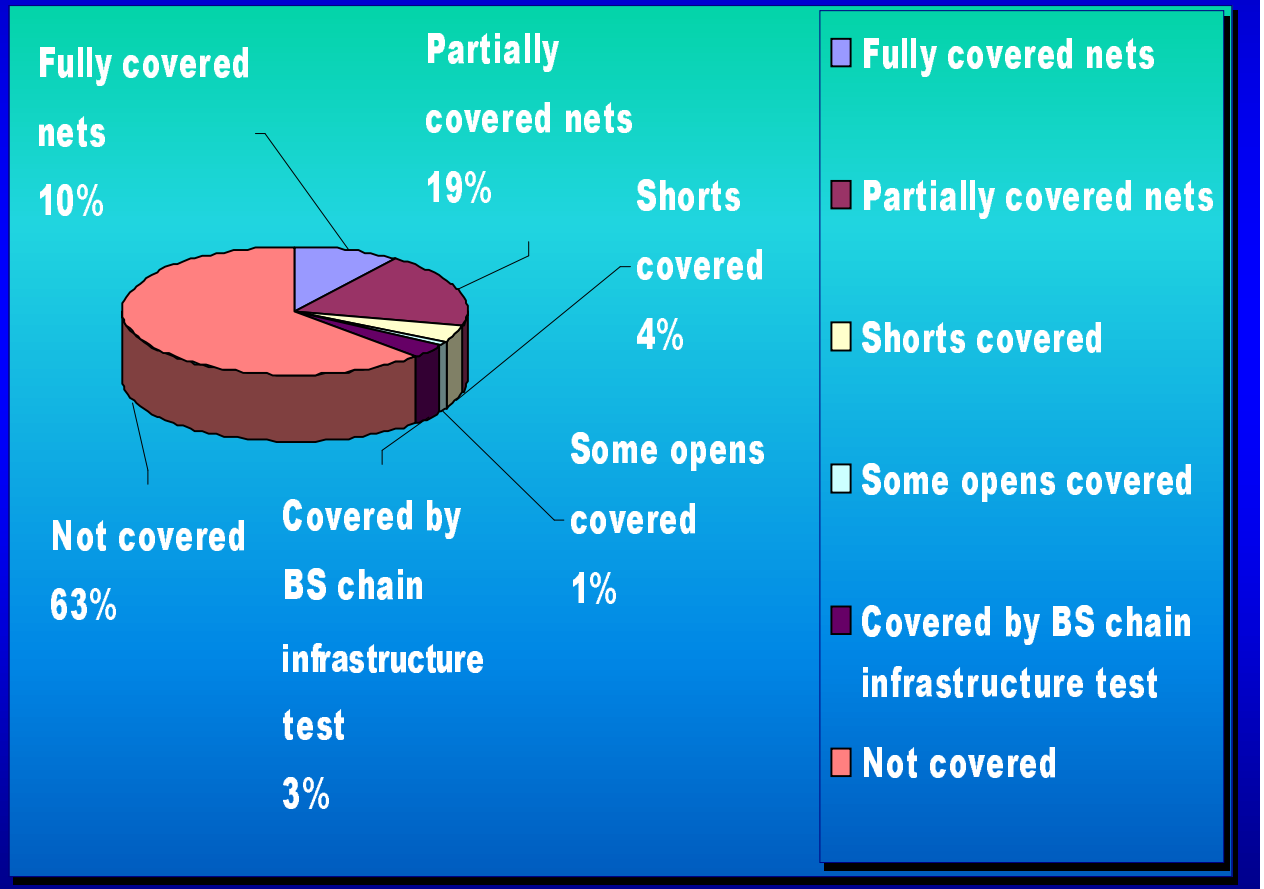
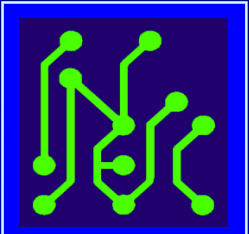
Testing the BSC Board - I

- The BS chain, the BS interconnections and some logic clusters are tested using boundary scan.
- A global testability of 37% is achieved for the interconnections.





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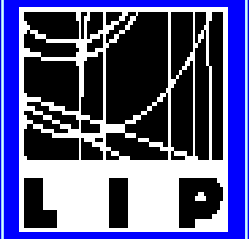

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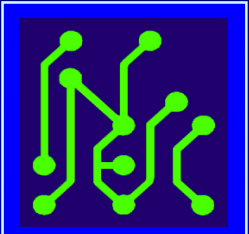
Testing the BSC Board - II

- The fault coverage was increased using a cluster test for the memories, the board base address and the test clock generator.



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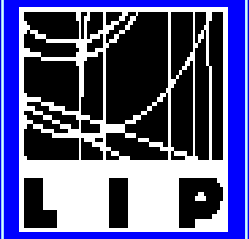

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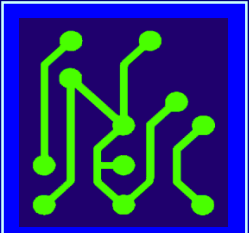
Conclusions & Future Work

- BSC board test and debug:
  - A fault coverage of 37% was achieved only for the interconnections.
  - The fault coverage was increased by the use of a cluster test to test non-BS circuitry.
  - Extensive debug of the BSC board logic was achieved using boundary scan.



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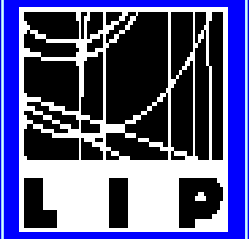

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Conclusions & Future Work

- The boundary scan test could be more efficient if BS circuits were used to interface the VME connectors.
- The utilisation of the unused PLD pins as additional BS test points is being evaluated.
- The application of tests through the MTM bus has not been done - so far tests were applied to the external JTAG port.