Fast and Low-Area TPGs Based on T-type Flip-Flops Can Be Easily Integrated to the Scan Path

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Abstract

A new structure of the fast and low-area test pattern generator (TPG) based on a linear register composed of T-type flip-flops that can be easily integrated with the scan path is proposed in the paper.

Nowadays, the techniques of incorporating TPGs containing T-type flip-flops in scan path either use asynchronous set and reset inputs of flip-flops or require adding a large amount of logic to transform TPG into the shift register. They all introduce a large area overhead and degrade timing parameters of TPG.

The area overhead of a new TPG structure is much less than in the case of to-day existing solutions. Moreover, it posses better timing parameters than conventionally designed TPGs. This last feature has been partially achieved due to the use of dedicated T-type flip-flops. The design of such flip-flop is comprised in the paper. In addition, authors propose a testing method that is suitable for verifying correct functioning of both the scan-path and the new type TPGs incorporated in it.

1. Introduction

New linear registers composed of T-type flip-flops, which are henceforth called T-FSRs, have lately gained a great popularity as effective test pattern generators (TPGs) for both static and timing faults in ASICs. Randomness of test patterns produced by the new type registers is similar like in the case of Cellular Automata [4, 5]. Moreover, such registers can also act as weighted random test pattern generators [8]. In addition to high fault coverage and relatively short testing time provided by the new type TPGs, their other advantages are low area overhead and high operating speed [4, 5]. This latter feature is particularly important when TPGs are used for at-speed testing of VLSI circuits manufactured in submicron technology. In order to achieve high operating frequency the new type register has to be constructed using special carefully designed T-type flip-flops, whose area and propagation delay are similar to those of D-type flip-flops coming from the same standard cell library.

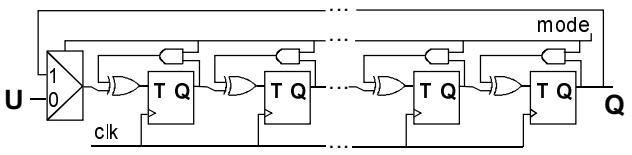

Fig. 1. Structure of T-FSR register composed of configurable T-type flip-flops.

The main drawback of the registers containing T-type flip-flops is difficulty with setting their initial state. They display also another disadvantage - the binary stream that is serially shifted into the *n*-bit register containing T-type flip-flops does not appear in the same form at its serial output with *n* clock cycles delay. The above two negative features of new type TPGs make it difficult to incorporate them into scan-paths in ASICs.

A way to work around the first of above disadvantages is to use the T-type flip-flops with asynchronous Set and Reset inputs. However, this increases the area overhead and decreases the operating frequency of TPG because the area and propagation delay of such flip-flops are larger than in the case of the devices with no asynchronous inputs.

In the case when a TPG containing T-type flip-flops is a part of a scan-path, it is usually being equipped with some extra hardware that transforms it to the shift register during scan mode. This facilitates setting its initial state (seeding) and allows for an undisturbed transfer of serial testing data through TPG. An exemplary schematic of such a TPG is shown in Figure 1. Two gates – AND and XOR – are added to each T-type flip-flop in order to transform it into D-type flip-flop operating in scan mode. These additional gates essentially increase the register complexity. Moreover, some propagation delay introduced by the multiplexer and XOR gate that are connected in series to the input of the first flip-flop in the register limits the maximal operating frequency of such TPG.

As it has been shown above, the means that are nowadays undertaken in order to facilitate T-FSR seeding and its incorporation in a scan-path make it impossible to exploit such advantages of this register as its low area overhead and high operating speed.

In the paper, a new design of T-FSR register is proposed that eases its integration with a scan-path preserving, at the same time, its all advantages. The *n*-bit T-FSR is equipped with a quasi-scan operating mode in which it implements a polynomial of the form $p(x) = x^n$. It is proven in the paper that a *n*-bit T-FSR, while it is in quasi-scan mode, can be set to an arbitrary initial state by *n*-bit sequence applied to its serial input. It is also shown that any *k*-bit sequence that is applied to the serial input of T-FSR that is in quasi-scan mode appears at its serial output with *n* clock cycles delay.

As it has been mentioned before, in order to achieve high operating frequency of T-FSR, the dedicated T-type flip-flops have to be used to construct the register. The design of such type flip-flop is also included in the paper. It posses better timing parameters and occupies lower silicon area than T-type flip-flops that are available in commonly used standard cell libraries.

The most common testing strategies comprise testing of the scan-path before it is used to apply testing stimulus to the CUT and capture testing responses of this latter. Unfortunately, serial test patterns that are usually used for testing of the scan-path are not suitable for testing T-FSRs. In the paper a new serial test pattern that checks correct operation in quasi-scan mode of all T-FSRs incorporated in the scan-path is developed. This pattern verifies the proper operation of the scan-path as well.

The rest of the paper is organised as follows. In Section 2, an overall idea of T-FSR quasi-scan mode is explained. Section 3 contains an algebraic description of T-FSR operation in quasi-scan mode. Section 4 presents methods of T-FSR designing and its integration with the scan-path. The design of the dedicated T-type flip-flop is included in section 5. Section 6 comprises the method of testing of T-FSR. Conclusions are encompassed in Section 7.

2. Idea of quasi-scan mode in T-FSR register

The schematic of a 4-bit T-FSR register equipped with quasi-scan mode capability is shown in Figure 2. It has the serial input SI, at which an input bit sequence U is applied, and the serial output, where an output bit sequence Q appears. The state diagram of this register takes a characteristic binary tree form when the serial input has either constant value 0 or constant value 1, as it is shown in Figure 3. The hexadecimal numbers in vertexes in both graphs denote the current state (contents) of the exemplary T-FSR.

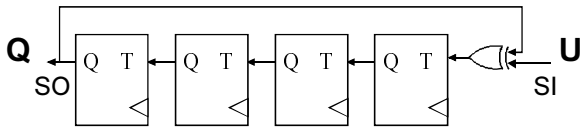

Fig. 2. Exemplar 4-bit T-FSR working in quasi-scan mode

Analysis of the graphs in Figure 3 leads to the following observations. Firstly, when constant value 0 is applied to the serial input of the exemplary T-FSR register this latter is set to 0 state after at most 4 clock cycles, regardless of its initial state. Moreover, after applying a certain sequence U to the serial input of T-FSR, the register always enters the same state corresponding to this input sequence, regardless of its initial state. For example, the T-FSR in Figure 2 enters always state <0100> after applying the sequence U=<0101> to its serial input. Other observation is that any *k*-bit input sequence of the exemplary T-FSR appears at its output with 4 clock cycles delay, similarly like it is in the case of a plain 4-bit shift register.

The above features apply to all T-FSRs that implement polynomial of the form $p(x)=x^n$, what will be proven in the next section. It is also shown in Section 4 that each T-FSR register composed of $n=2^k$ T-type flip-flops, where k=0, 1, 2, ... , implements polynomial of the form $p(x)=x^n$, where $n=2^k$.

The main advantage of the T-FSR shown in Figure 2, (as compared to that presented in Figure 1) is its reduced area overhead.

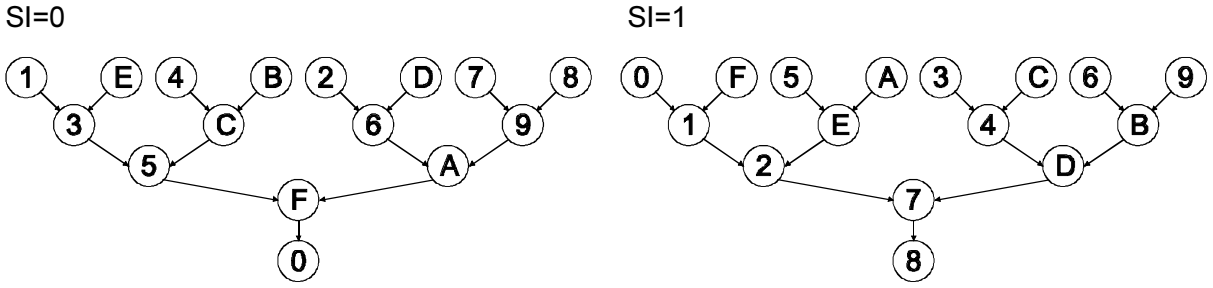

Fig. 3. State diagrams of 4-bit T-FSR for SI=0 and SI=1

3. Algebraic description of T-FSR working in quasi-shift mode

Operation of a *n*-bit T-FSR during *m* clock cycles is defined by equation 1 [6, 7].

$$[u(x)+x^m h(x)]/p(x)=q(x)+r(x)/p(x), \quad (1)$$

where:

$u(x)$ is a polynomial corresponding to binary stream U that is applied to the input SI of the register; *deg u(x)=m-1*,

$h(x)=\sum_{i=0}^{n-1} \oplus g_i (1+x)^i$ is a polynomial that contains bits g_i (*i=0, 1, ..., n-1*) of initial state G of the register; *deg h(x)=n-1*,

$r(x)=\sum_{i=0}^{n-1} \oplus s_i (1+x)^i$ is a polynomial equal to the reminder of division 1, which contains bits s_i (*i=0, 1, ..., n-1*) of final state S of the register; S is called a signature; *deg r(x)=n-1*,

$p(x)=1+(1+x)^n$ is a characteristic polynomial of the register (it is a divisor in equation 1), *deg p(x)=n*,

$q(x)$ is a polynomial equal to the quotient of division 1; *deg q(x)=m-1*.

Definition 1

The *n*-bit T-FSR is said to be working in the quasi-scan mode when it implements polynomial $p(x)=x^n$.

□

The following theorems describe properties of T-FSRs working in the quasi-scan mode.

Theorem 1

Any *n*-bit T-FSR working in the quasi-scan mode can be set to arbitrary state $S=s_0 s_1 ... s_i ... s_{n-2} s_{n-1}$, regardless of its initial state G by applying *n*-bit sequence $u(x)=\sum_{i=0}^{n-1} \oplus s_i (1+x)^i$ to its serial input.

Proof:

Taking into account that $m=n$ and $p(x)=x^n$ equation 1 takes the following form:

$$u(x)/x^n+h(x)=q(x)+r(x)/x^n \quad (2)$$

Multiplying both sides of equation 2 by x^n and rearranging the results in:

$$x^n[q(x)+h(x)]=u(x)+r(x) \quad (3)$$

Taking into account that $deg[u(x)+r(x)] < n$ and $deg[x^n(q(x)+h(x))] \geq n$ leads to:

$$u(x)+r(x)=0 \Leftrightarrow u(x)=r(x)=\sum_{i=0}^{n-1} s_i (1+x)^i \quad \square$$

Corollary 1

Any *n*-bit T-FSR working in quasi-scan mode is zeroed, regardless of its initial state G, after $z \geq n$ clock cycles, provided that its serial input has constant value 0 during this period.

Example 1

The bit sequence *u(x)* is to be found that sets T-FSR in Figure 2 to state S=0010. The values of signature bits are $s_0=0$, $s_1=1$, $s_2=0$, $s_3=0$. According to theorem 1:
$u(x) = 0(1+x)^0 + 0(1+x)^1 + 1(1+x)^2 + 0(1+x)^3 = 1+x^2$.
Thus U=1010.

Theorem 2

Any *k*-bit input sequence $A=a_0 a_1 a_2 ... a_i ... a_{k-2} a_{k-1}$ of *n*-bit T-FSR that is working in quasi-scan mode appears at its serial output in the same form with *n* clock cycle delay.

Proof:

In order to transfer the whole *k*-bit sequence A from the serial input of *n*-bit T-FSR working in the quasi-scan mode to its serial output, the register has to be clocked $m=n+k$ times. The whole *m*-bit input sequence *u(x)* of this T-FSR can be written as follows: $u(x)=u'(x)+x^n a(x)$, where $a(x)=\sum_{i=0}^{k-1} a_i x^i$, $deg\ a(x)<k$, $deg\ u'(x)<n$.

Similarly, the output sequence of the register can be written in the form: $q(x)=b(x)+x^k q'(x)$, where $deg\ b(x)<k$, $deg\ q'(x)<n$. The bit sequence *b(x)* is the sequence appearing at the serial output of the T-FSR *n* clock cycles after sequence *a(x)* is applied to the serial input of the register. Under above assumptions and taking in account that $p(x)=x^n$, equation 1 takes the following form:

$$[u'(x)+x^n a(x)+x^{n+k} h(x)]/x^n=b(x)+x^k q'(x)+r(x)/x^n \quad (4)$$

Multiplying both sides of the above equation by x^n and appropriate grouping of the polynomials according their degree gives:

$$x^{n+k}[q'(x)+h(x)]+x^n[a(x)+b(x)]+[u'(x)+r(x)]=0 \quad (5)$$

Because $deg\ x^{n+k}[q'(x)+h(x)] \geq n+k$, $n > deg\ u'(x)+r(x)$ and $n+k > deg\ x^n[a(x)+b(x)] \geq n$, the following equality is satisfied $a(x)+b(x)=0 \Leftrightarrow a(x)=b(x)$. □

4. Designing T-FSRs equipped with quasi-scan mode

T-FSRs that are particularly useful for implementing quasi-scan mode are those composed of $n=2^k$ flip-flops, where *k=0, 1, 2, ...* The following theorem applies to them.

Theorem 3

The *n*-bit T-FSR implements polynomial $p(x)=x^n$ if $n=2^k$, where *k=0, 1, 2, ...*

Proof:

Assuming that $n=2^k$, where $k=0, 1, 2, ...$, the characteristic polynomial $p(x)$ of n-bit T-FSR can be transformed to the following form:

$$p(x) = 1 + (1+x)^n = 1 + (1+x)^{2^k} = 1 + 1 + x^{2^k} = x^{2^k} = x^n \quad \square$$

According to the above theorem, any n-bit T-FSR, where $n=2^k$ and $k=0, 1, 2, ...$, works in quasi-scan mode. Moreover, any register composed of such T-FSRs connected in series works in quasi-scan mode, as well. Henceforth, the T-FSR composed of 2^k T-type flip-flops, where $k=0, 1, 2, ...,$ will be denoted as T-QSR (this abreviation stands for Quasi Shift Register composed of T-type flip-flops).

Theorem 4

The n-bit T-FSR composed of r T-QSRs connected in series, each of which has length 2^{k_i}, where $k_0, k_1, ..., k_{r-1} = 0, 1, 2, ..., k$ and $i=0, 1, ..., r-1$, implements polynomial $p(x)=x^n$.

Proof:

The polynomial implemented by a n-bit T-FSR composed of r T-QSRs connected in series, each of which has length 2^{k_i}, where $k_0, k_1, ..., k_{r-1} = 0, 1, ..., k$ and $i=0, 1, ..., r-1$, can be written as follows: $p(x) = \prod_{i=0}^{r-1} x^{a_i} = x^L$, where $a_i = 2^{k_i}$ and $L = \sum_{i=0}^{r-1} a_i$. Since L is the sum of the lengths of these registers $L=n$. Thus, $p(x)=x^n$.

Theorem 5

The n-bit T-FSR working in quasi-scan mode, where $2^{k-1} < n < 2^k$, can be constructed of $k \geq r \geq 2$ T-QSRs connected in series, each of which has length 2^{k_i} - where $k_0, k_1, ..., k_{r-1} \in \{0, 1, 2, ..., k\}$, $k_i \neq k_j$ for $i \neq j$ and $i, j = 0, 1, ..., r-1$.

Proof:

The number n of T-type flip-flops in the T-FSR register can be represented as follows: $n = \sum_{j=0}^{k-1} b_j 2^j$, where $b_j=1$ means that T-QSR of the length 2^j is a part of n-bit T-FSR and $b_j=0$ means that it is not. $\square$

Theorems 4 and 5 are fundamental for the method of constructing T-FSR registers of arbitrary length equipped with quasi-scan mode. An overall structure of such n-bit register is presented in Figure 4. The meaning of coefficients $b_0, b_1, ..., b_{k-1}$ is the same as in theorem 5. The n-bit T-FSR has two operating modes: normal (mode=0) and quasi-scan (mode=1). T-type flip-flops form one $(n-1)$-bit ring in normal mode, while in quasi-scan mode the whole register is composed of r T-QSRs connected in series, each of which is working in quasi-scan mode. Notice that maximal operating frequency of the T-FSR in Figure 4, when it is working in normal mode, is higher than in the case of the register shown in Figure 1. It is limited by propagation delay of the multiplexer presented in the main feedback loop of the T-FSR, which is smaller than the propagation delay introduced by the connected in series multiplexer and XOR gate that are present in the main feedback loop of the register in Figure 1. The above advantage is achieved at the cost of necessity of using T-FSR that length is one bit larger than the number of the inputs of the CUT. Moreover, a T-FSR working in quasi-scan mode has to be clocked with lower frequency than in the normal operating mode. It is because the propagation delay of connected in series XOR and AND gates limits the operating frequency of the T-FSR in quasi-scan mode (see Figure 4).

The T-FSR illustrated in Figure 4 displays a considerable reduction in area overhead, in comparison with the register shown in Figure 1. Implementation of the scan mode in the register in Figure 1 requires n pairs XOR-AND gate and a multiplexer. In order to equip n-bit TPG based on T-FSR with quasi-scan mode at most $\lceil \log_2(n) \rceil$ pairs XOR-AND gate, a multiplexer and an additional T-type flip-flop (which area is approximately equivalent to area of one XOR-AND gate pair) are necessary.

In order to further increase the operating frequency and decrease the area overhead of the T-FSR the last mentioned has to be constructed with dedicated T-type flip-flops. The design of such flip-flop, which propagation delay time and area are essentially smaller than in the case of T-type flip-flops that can be found in commonly used standard cell libraries, is encompassed in the next section.

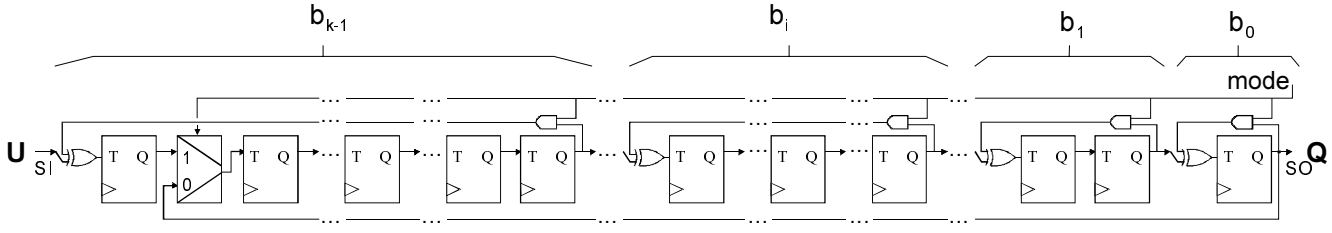

Fig. 4. The n-bit T-FSR equipped with quasi-scan mode

5. Dedicated T-type Flip-Flop in CMOS VLSI technology

In this chapter an example dedicated T-type flip-flop is presented, which has been designed under AMS 0.8 μm CMOS technology, [1], and it is here compared to the alternative 2 cell solution consisting of a D-type flip-flop and an Exclusive OR gate.

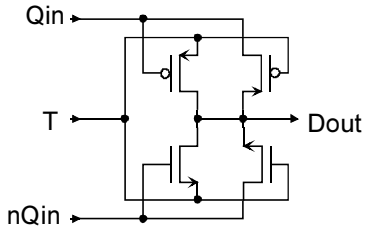

Fig. 5. The 4-transistor modification circuit.

The standard cell library in the AMS 0.8 μm CMOS technology offers both the D-type flip-flop (DF8 cell) and the Exclusive-OR gate (EO1 cell), but it does not offer any T-type flip-flops. The T-type flip-flop was developed from the existing D-type flip-flop, (DF8 cell), by adding a circuit shown in Figure 5. In fact, this simple 4-transistor circuit performs Exclusive-OR function on T (input) and Q (output) signals, but it is smaller and faster than a fully-featured Exclusive-OR library cell. This is possible, because inside a single cell both simple *Qin* and inverted *nQin* flip-flop's signals are internally accessible, and also an output buffer is not necessary for the Exclusive OR part.

The newly designed T-type flip-flop cell (let us call it TF8) was simulated under SpectreS analogue simulator, which is the standard analogue simulator in CADENCE VLSI design environment. The clock to output propagation times t_{pcqr} (for rising output signal) and t_{pcqf} (for falling output signal) were measured, and they appeared to be almost the same as in the original **D**-type flip-flop (DF8). For the simple (positive) Q output with a load capacitance C_{LOAD} = 0.3 [pF] the measured times were t_{pcqr} = 1.8 [ns], and t_{pcqf} = 1.65 [ns]. A difference was observed in the setup time t_{su}. The measured t_{su} was equal to 0.65 [ns] for the new T-type flip-flop, and 0.45 [ns] for the original D-type flip-flop. In order to easily interpret these values and compare the new T-type flip-flop to a D-type flip-flop with Exclusive-OR approach, the theoretical maximum operating frequency was defined.

For a single (D or T) Flip Flop the theoretical maximum operating frequency is defined as:

$$f_{\max} = \frac{1}{t_{su} + t_{pcq}}, \quad where \quad t_{pcq} = \max\{t_{pcqr}, t_{pcqf}\}$$

For 2 cells solution (D Flip Flop + Ex-OR gate) the theoretical maximum operating frequency equals:

$$f_{\max} = \frac{1}{t_{pd} + t_{su} + t_{pcq}}, \quad where \quad t_{pcq} = \max\{t_{pcqr}, t_{pcqf}\},$$

$$t_{pd} = \max\{t_{pdr}, t_{pdf}\}$$

Achieved results are gathered in Table I. Because the Ex-OR cell's delay depends on the connected load capacitance, which depends on placement and routing, the theoretical maximum operating frequency was calculated for 2 cases: random place & route (assuming C_{LOAD} = 0.3 [pF]), and optimised place & route (the **D** Flip Flop close to the Ex-OR cell and C_{LOAD} reduced to 0.03 [pF]), see results in the table.

Table I	Theoretical f_{max}	Chip Area
D Flip-Flop (DF8)	444 MHz	10 x A1
Dedicated **T** Flip-Flop	408 MHz	12 x A1
D Flip-Flop + Exclusive OR (optimised place & route)*	282 MHz 333 MHz*	16 x A1

In Table I, the chip area is expressed as a multiplicity of the unity area A1, which is characteristic for a given standard cell library (here A1= 186 μm^2).

The dedicated T-type flip-flop is at least 22% faster then the 2 cell solution, and it occupies only 75% of the chip area as required by the 2 cell approach.

6. Testing of the T-FSRs and the scan-path

In the most common testing strategies the scan-path is tested before it is used to apply testing stimulus to the CUT and capture testing response of this latter. This task is usually accomplished by a certain test pattern that is serially shifted through the scan-path. We assume that every TPG based on T-FSR is a part of the scan-path. Thus, the serial test pattern provided for the scan-path should also test all T-FSRs incorporated in it while they are working in quasi-scan mode.

Authors of the paper have found the seven-bit sequence ST_{DT}=1101000 that ensures exhaustive functional testing of both D-type flip-flops of the scan-path and T-type flip-flops of the T-FSRs, provided that these latter are initially zeroed. In order to check if all T-FSRs correctly operate in quasi-scan mode, sequence ST_{DT} needs to be immediately followed by the sequence $SZ(2^{max})$ of 2^{max} zeros, where 2^{max} is the length of the largest T-QSR incorporated in the scan-path. The sequence $SZ(2^{max})$ guaranties functional testing of the feedback loops of all T-QSRs which T-FSRs are composed of.

Verification of correct operation of the scan-path and all T-FSRs incorporated in it is done by checking if undisturbed concatenation of the sequences ST_{DT} and $SZ(2^{max})$ appears at the output of the scan-path.

Testing time, in turn, can be calculated as follows. Let us assume that there are s T-FSRs incorporated in the scan-path, each m_i long, where $i=1, 2, ..., s$. The total length of the scan-path, including the length of all T-FSRs contained in it, is n. Let $M=max(m_i \mid i=1, 2, ..., s)$ be the length of the largest T-FSR and 2^{max} be the length of the largest T-QSR that are contained in the scan-path. Time that is necessary to test the scan-path and all incorporated in it T-FSRs using the concatenations of the sequences ST_{DT} and $SZ(2^{max})$ equals to: $\tau_{test} = M+7+2^{max}+n$.

Zeroing of all T-FSRs occurs during the first M clock cycles of the testing procedure. During the next $7+2^{max}$ clock cycles the bit sequences ST_{DT} and $SZ(2^{max})$ are applied one after another to the input of the scan-path. The last n clock-cycles operate to shift these both sequences out of the scan-path.

Notice that making the T-FSR zeroed requires that its serial input has to be fed through the AND gate. Moreover, every T-FSR incorporated in the scan-path has to be kept in zero state until the first bit of ST_{DT} sequence arrives to its serial input.

7. Conclusions

In the paper an original method of designing TPGs, which are based on linear registers composed of T-type flip-flops and which can be easily integrated with scan-path, is proposed. The TPG is equipped with quasi-scan mode in addition to its normal operation mode. When the n-bit TPG is in quasi-scan mode its internal state can be easily set by applying a n-bit sequence to its serial input, similarly like it is in the case of a conventional n-bit shift register. Moreover, such TPG transfers any bit sequence from its serial input to its serial output in an undisturbed form, just delaying it by n clock cycles. The above two features make integration of the new type TPG with the scan path easy.

Contrary to the traditional techniques facilitating incorporation of TPG in scan path, which use asynchronous inputs of flip-flops or require large amount of additional logic to transform all T-type flip-flops in the register to D-type ones, the area overhead introduced by the new method is low. Moreover, the new TPG structure that is proposed in the paper posses better timing parameters than conventional solutions, what makes it particularly useful for at-speed testing. Using the dedicated T-type flip-flop to construct the new type TPG has essential impact on achieving the low area and high speed of operation of this latter. T-type flip-flops that are available in the standard cell libraries are usually composed of D-type flip-flop and two-input Exclusive-OR gate. The design of the T-type flip-flop proposed in the paper is at least 22% faster and occupies 25% less silicon area than the standard two-cell solution.

The test method that can verify correct operation in quasi-scan mode of the single T-FSR as well as the whole scan-path, which incorporates several T-FSRs, is developed in the paper, too. It is based on functional testing – so it can be used to verify proper operation of the scan-path and T-FSRs that are manufactured in arbitrary technology. Another advantage is its relatively short testing time.

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