Fast and Low-Area TPGs Based On T-type Flip-Flops Can Be Easily Integrated to the Scan Path

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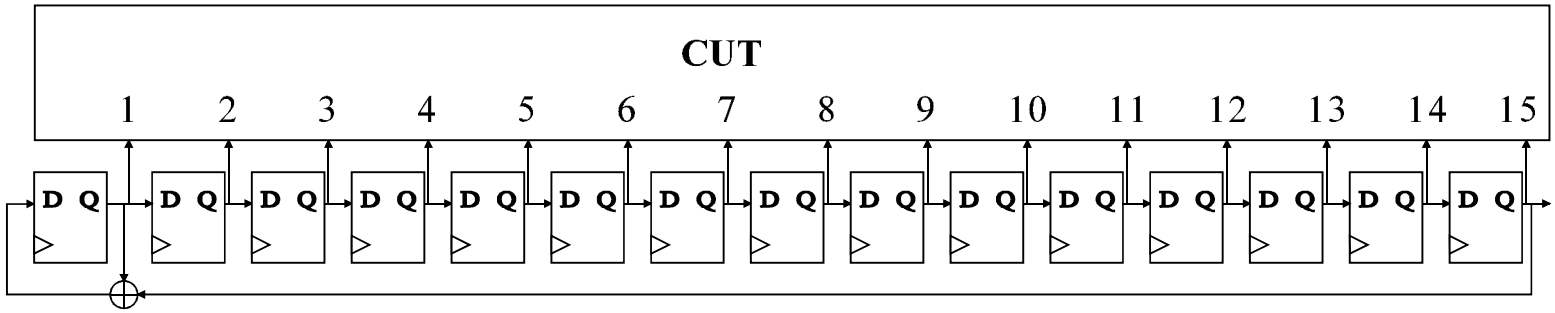
Outline

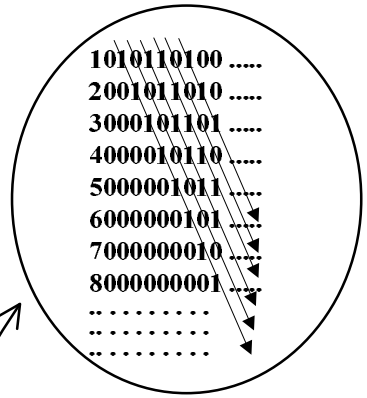
- Advantages of TPG based on T-type flip-flops
- Idea of dedicated T-type flip-flop
- Problems with seeding of TPG based on T-type flip-flops
- Idea of T-QSR and its application to solving the above issues
- Advantages of T-QSR
  - easy reseeding
  - quasi scan mode
- TPG composed of T-QSRs and its testing
- Comparison of presented solutions
- Conclusions

What is wrong with a plain LFSR ?



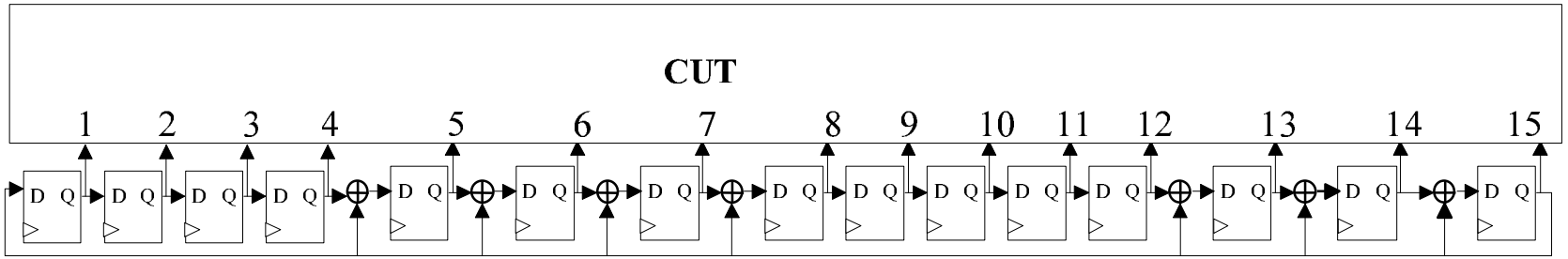
$$p(x)=1+x^{14}+x^{15}$$

Consecutive test patterns
at the outputs of this LFSR
are
strongly cross-correlated !



Existing solutions

LFSR with many XOR gates in internal feedback loop



$$p(x)=1+x^4+x^5+x^6+x^7+x^{12}+x^{13}+x^{14}+x^{15}$$

The cross-correlation of consecutive patterns generated by this LFSR is **WEAKER** than in the previous case but the above solution is **MORE EXPENSIVE** !

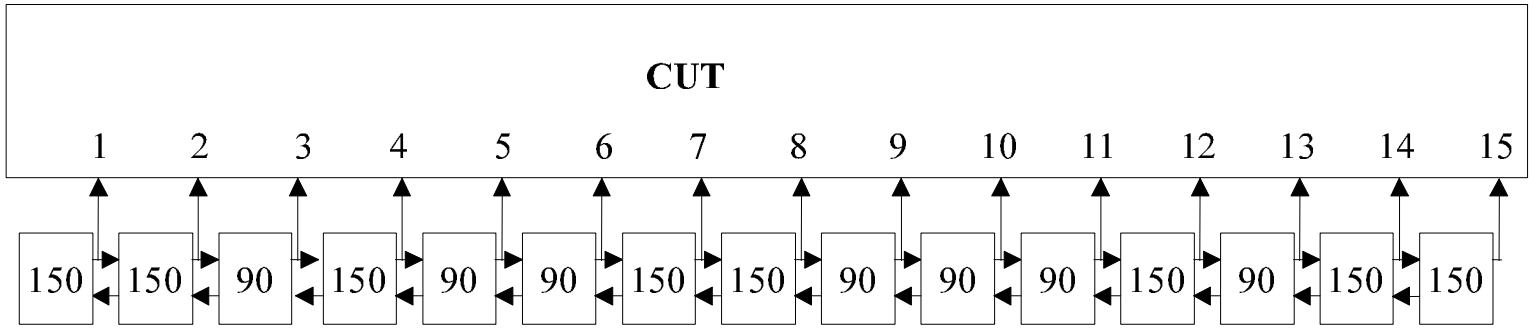
Existing solutions

Cellular Automata

[Hortensius at all, '89]

cells 90 are based on D-FF

cells 150 are based on T-FF



$$p(x)=1+x^{14}+x^{15}$$

The cross-correlation between consecutive patterns at the outputs of CA is **VERY WEAK** but it is rather **EXPENSIVE** test pattern generator

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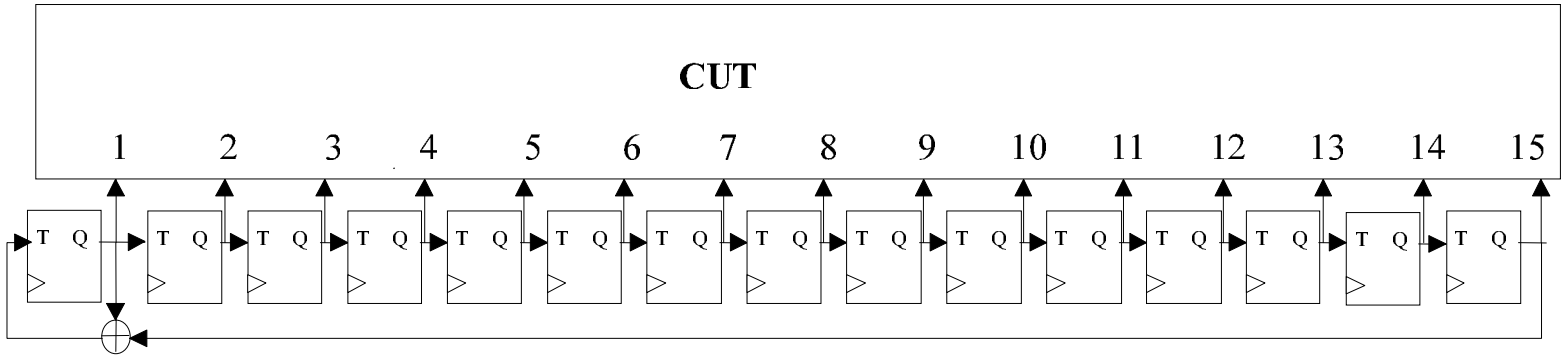
Existing solutions

LFSR with all T-type flip-flops

[Yarmolik & Murashko, '95]



$$p(x)=1+x+x^3+x^5+x^7+x^9+x^{11}+x^{13}+x^{15}$$

This register also generates patterns
that are **VERY WEAKLY** cross-correlated

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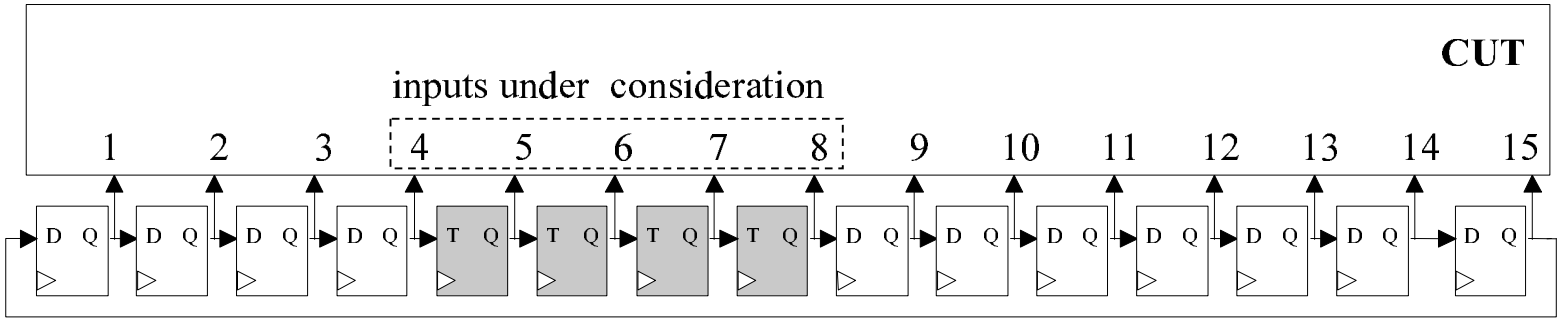
Existing solutions

DT-LFSR : LFSR with D and T flip-flops

[Hławiczka, ’92; Garbolino & Hławiczka, ETW’99, EDCC-3‘99]



$$p(x)=1+x^{14}+x^{15}$$

Patterns generated by this register are
VERY WEAKLY cross-correlated at the points
we really need this

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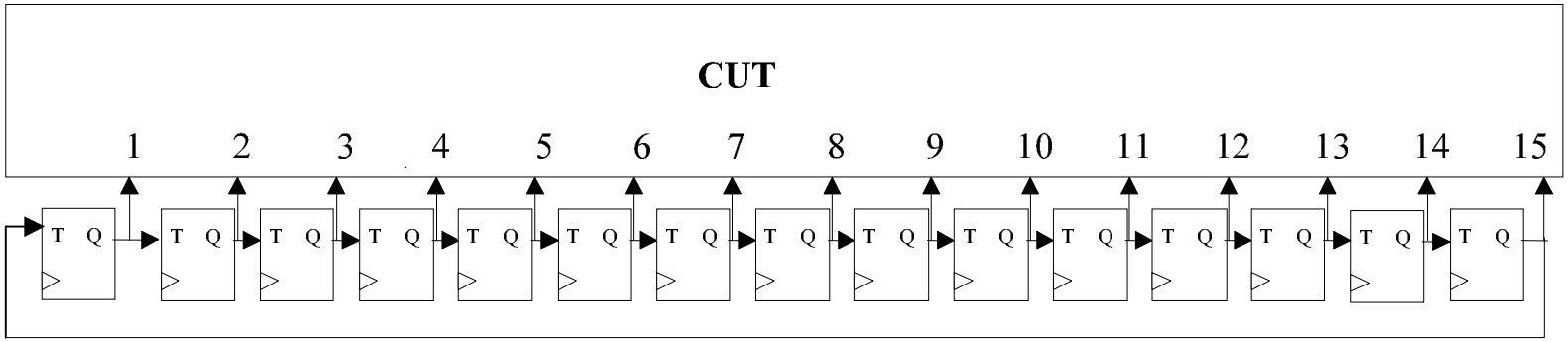
Existing solutions

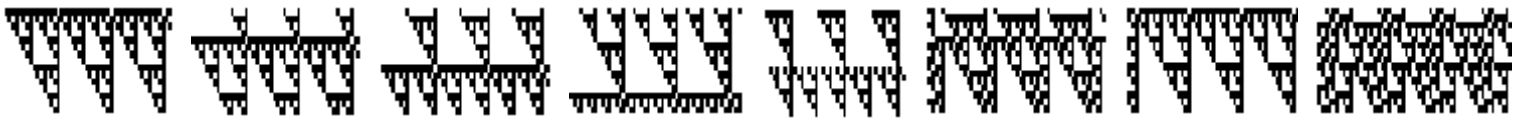
T-FSR : TPG in the form of ring composed of T-type flip-flops

[Novak, ETW '99, EDCC-3 '99]



$$p(x)=x+x^2+x^3+x^4+x^5+x^6+x^7+x^8+x^9+x^{10}+x^{11}+x^{12}+x^{13}+x^{14}+x^{15}=(1+x)^{15}$$

This solution is relatively **CHEAP** and generates **VERY WEAKLY** cross-correlated **WEIGHTED** random patterns !!!



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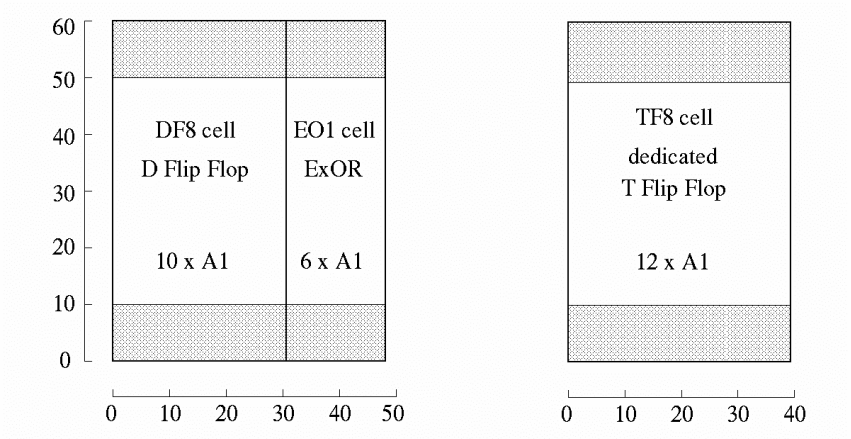
Idea of dedicated T-type flip-flop

Comparison of cells area of classical and dedicated T-type flip-flop

AMS Standard Cell Library
0.8 μ m Double-Metal CMOS 5V



A1=186 μm

	f_{max}	Area
D Flip-Flop (DF8)	444 MHz	10 x A1
Dedicated **T** Flip-Flop	408 MHz	12 x A1
D Flip-Flop + Exclusive OR	282 MHz	
(optimised place & route)*	333 MHz*	16 x A1

Dedicated T-type flip-flop is about **22% faster** and occupies **25 % less area** than 2 cell solution (D-FF+XOR)

Moreover, its maximal operating frequency is **only 9% lower** and its area is **only 20% larger** than in the case of D-type flip-flop

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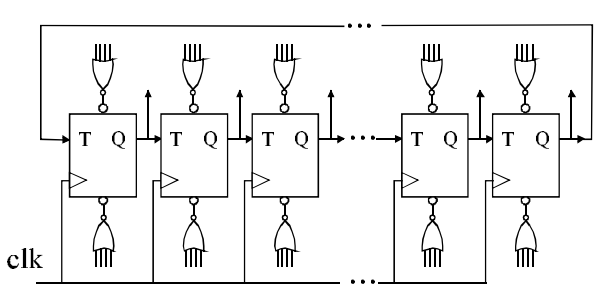
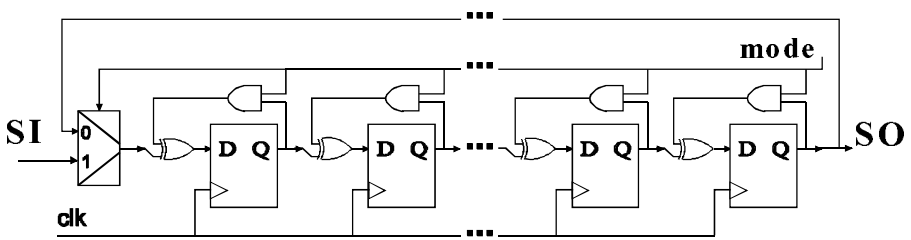
Problems with T-FSR seeding
Existing solutions

TPG based on dedicated T-type flip-flops with set and/or reset inputs.



TPG based on classical T-type flip-flops, which is transformed to shift register in scan mode.



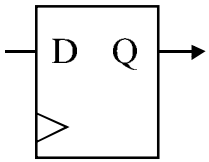
mode: 1 - scan mode, 0 - T-FSR TPG

DISADVANTAGES:

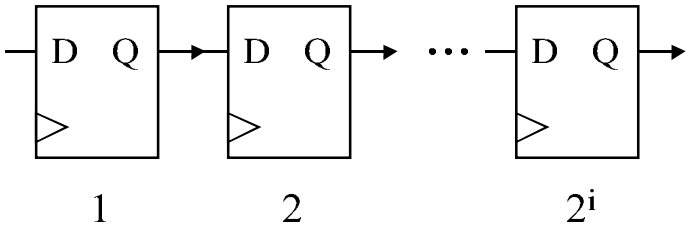
- high area overhead
- advantages of dedicated T-type flip-flop cannot be fully exploited

Idea of Quasi Shift Register composed of T-type flip-flops : T-QSR

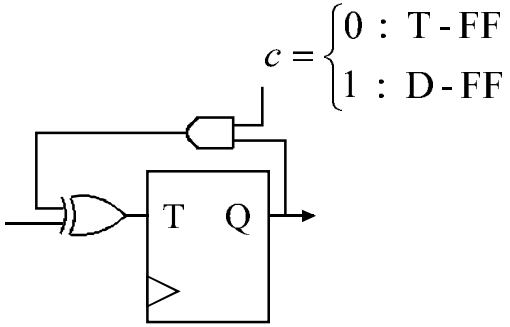
T-QSR has the same polynomial $p(x)=x^n$ like n-bit shift register



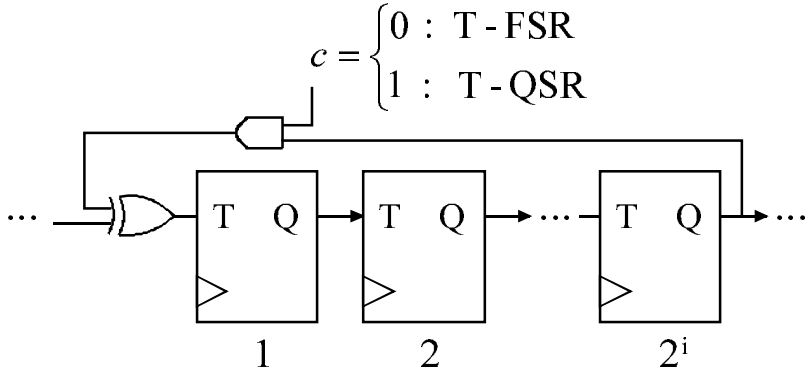
$p(x)=x$



$p(x)=x^n,\ n=2^i$



$p(x) = 1+(1+x) = x$



$p(x) = 1+(1+x)^n = x^n,\ n=2^i$

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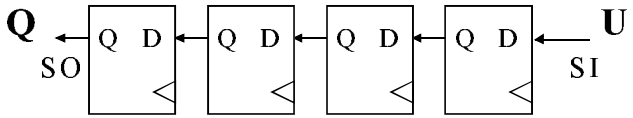
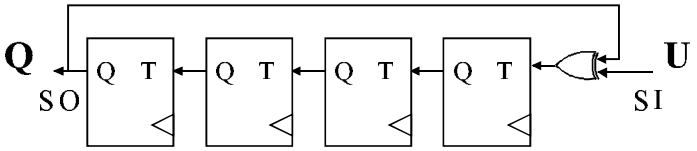
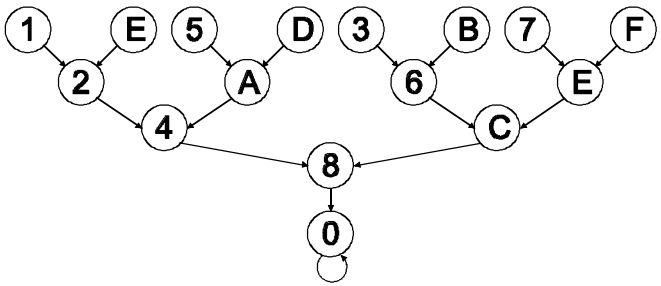
Behaviour of T-QSR is similar to shift register

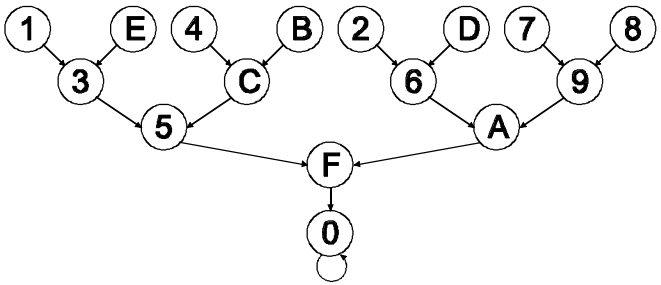




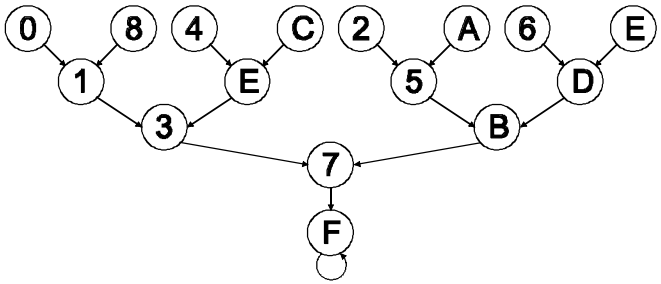
SI=0



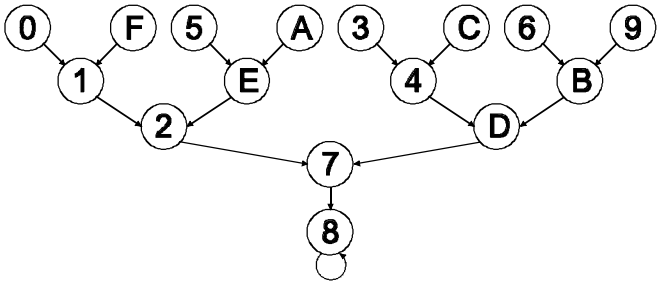
SI=0



SI=1



SI=1



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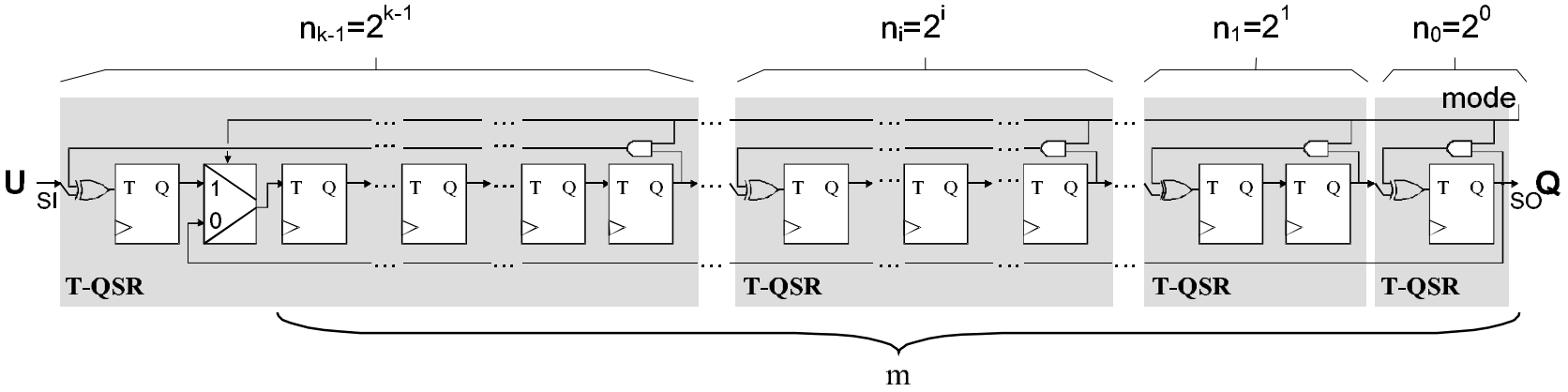
The m-bit T-FSR equipped with quasi-scan mode



$$m+1=\sum_{i=0}^{k-1} n_i b_i, \quad \mathrm{b_i} \in \{0,1\}, \quad \mathrm{n_i} = 2^i$$

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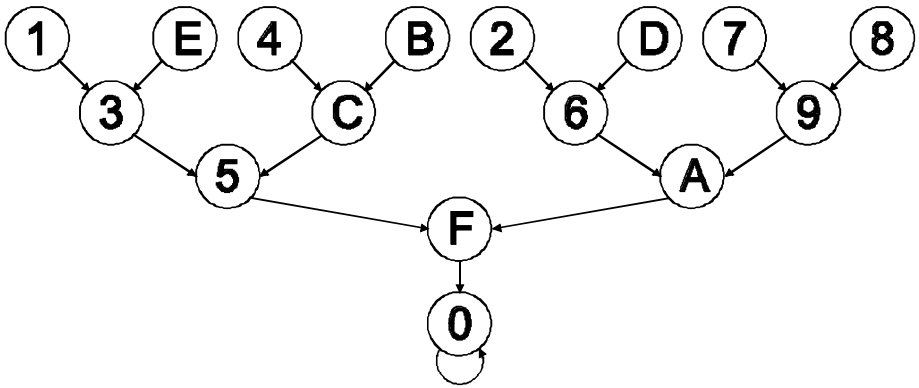
Resetting of T-QSR

SI=0



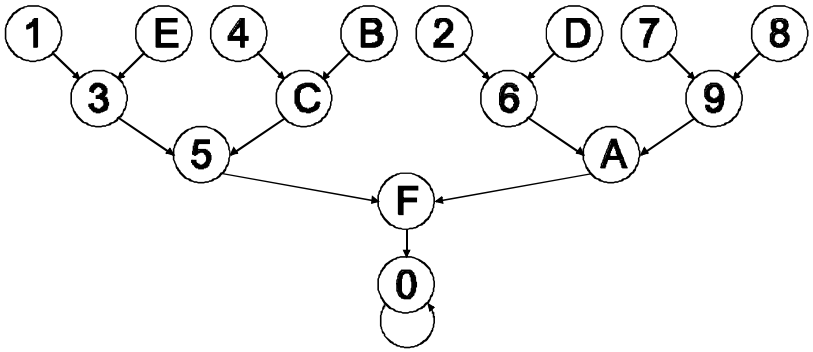
The **4**-bit T-FSR register
has a tree-like state diagram,
what makes possible to reset
this register in **4** clock cycles

Any T-FSR of the length $\mathbf{n=2^k}$
has a tree-like state diagram,
and can be reset in **n** clock cycles

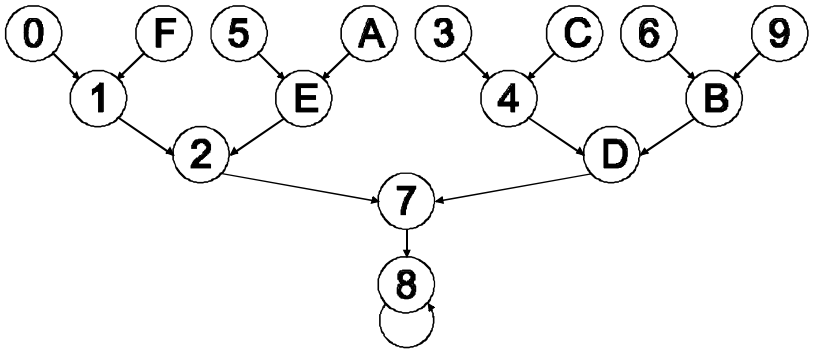
Setting T-QSR to an arbitrary state

Any state can be reached in 4 clock cycles

SI=0

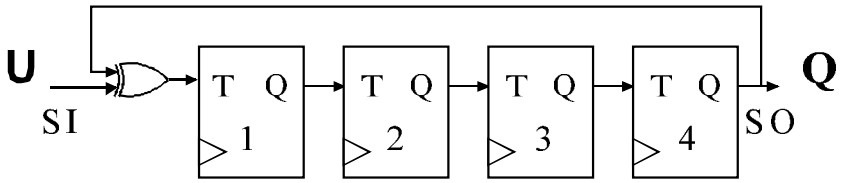


SI=1



SI=1000 → F(1111)

Idea of quasi-scan mode for T-QSR



SI	Q_1	Q_2	Q_3	Q_4	SO	
1	0	0	0	0	**0**	
0	1	0	0	0	**0**	
0	1	1	0	0	**0**	n=4
1	1	0	1	0	**0**	
1	0	1	1	1	**1**	
0	0	1	0	0	**0**	
0	0	1	1	0	**0**	
0	0	1	0	1	**1**	
0	1	1	1	1	**1**	
0	0	0	0	0	**0**	
0	0	0	0	0	**0**	
0	0	0	0	0	**0**	
0	0	0	0	0	**0**	

Any input sequence is repeated at the output of a $n=2^i$ bit T-QSR with n clock cycles delay, though it is processed in the register

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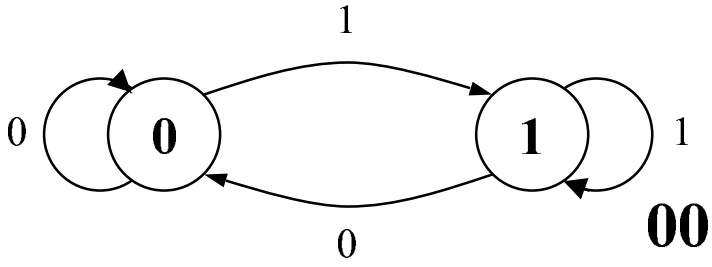
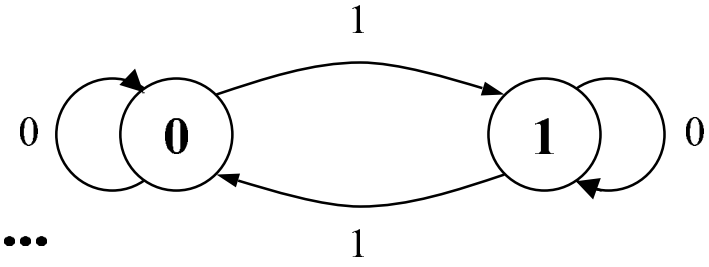
Testing of T-type flip-flop

D-type flip-flop

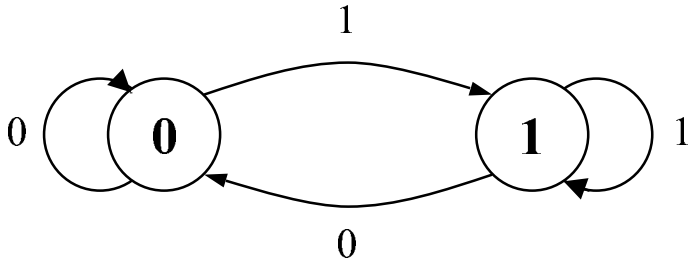


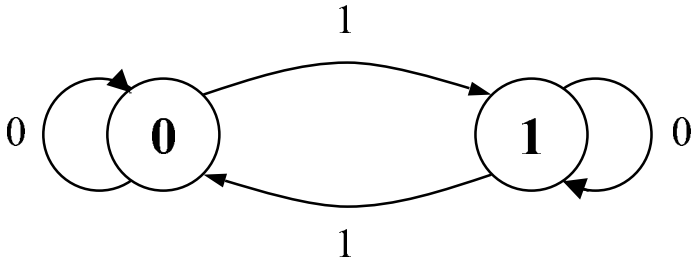
T-type flip-flop



001100...

Sequence **001100...** tests **D-FF** but doesn't test **T-FF**





1101000

Sequence **1101000** tests both **D-FF** and **T-FF**

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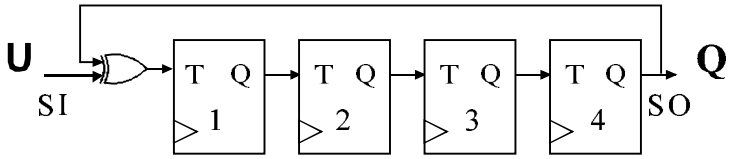
Testing of T-QSR

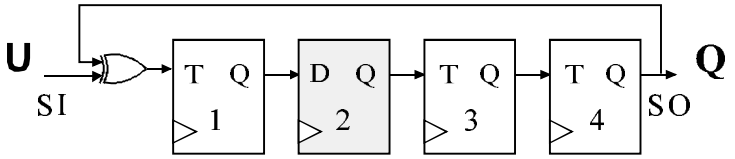
Functional test for T-type flip-flops in T-QSR

Fault free circuit



SI	Q_1	Q_2	Q_3	Q_4	SO
1	0	0	0	0	0
1	1	0	0	0	0
0	0	1	0	0	0
1	0	1	1	0	0
0	1	1	0	1	1
0	0	0	1	1	1
0	1	0	1	0	0
0	1	1	1	1	1
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0

Fault: 2nd flip-flop behaves like D-type one



SI	Q_1	Q_2	Q_3	Q_4	SO
1	0	0	0	0	0
1	1	0	0	0	0
0	0	1	0	0	0
1	0	0	1	0	0
0	1	0	1	1	1
0	0	1	1	0	0
0	0	0	0	1	1
0	1	0	0	0	0
0	1	1	0	0	0
0	1	1	1	0	0
0	1	1	0	1	1

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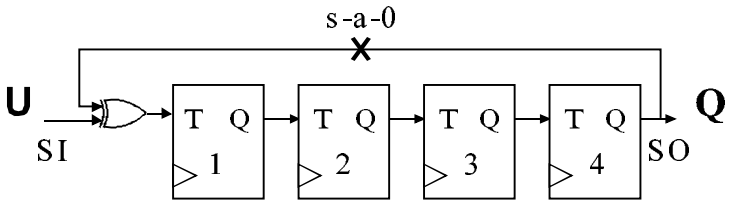
Testing of T-QSR

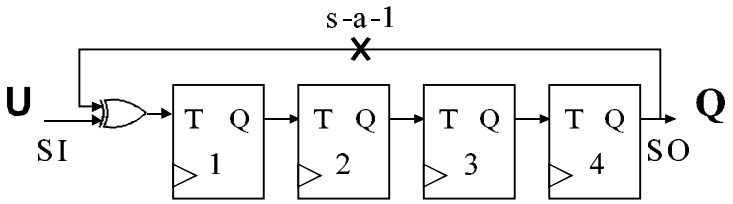
Functional test for s-a-x fault in feedback loop of T-QSR

Fault: stuck-at-0



SI	Q_1	Q_2	Q_3	Q_4	SO
1	0	0	0	0	0
1	1	0	0	0	0
0	0	1	0	0	0
1	0	1	1	0	0
0	1	1	0	1	1
0	1	0	1	1	1
0	1	1	1	0	0
0	1	1	0	1	1
0	1	0	1	1	1
0	1	1	1	0	0
0	1	0	0	1	1

Fault: stuck-at-1



SI	Q_1	Q_2	Q_3	Q_4	SO
1	0	0	0	0	0
1	0	0	0	0	0
0	0	0	0	0	0
1	1	0	1	0	0
0	1	1	1	1	1
0	0	0	0	0	0
0	1	0	0	0	0
0	0	1	0	0	0
0	1	1	1	0	0
0	0	0	0	1	1
0	1	0	0	1	1

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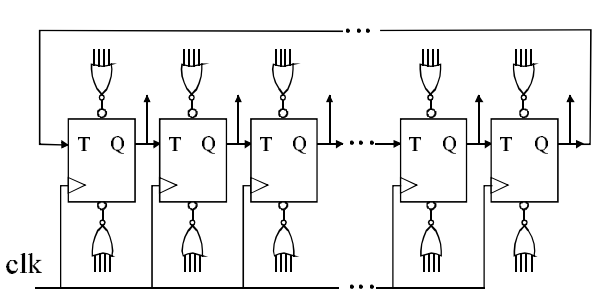
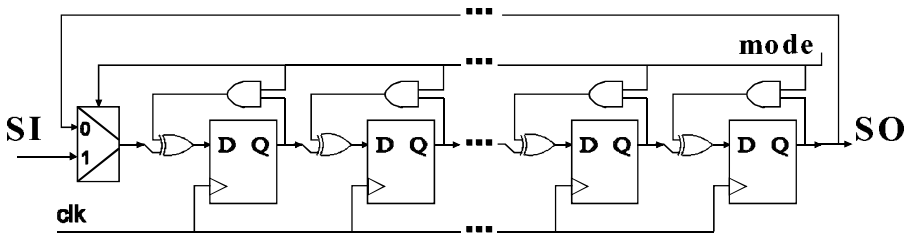
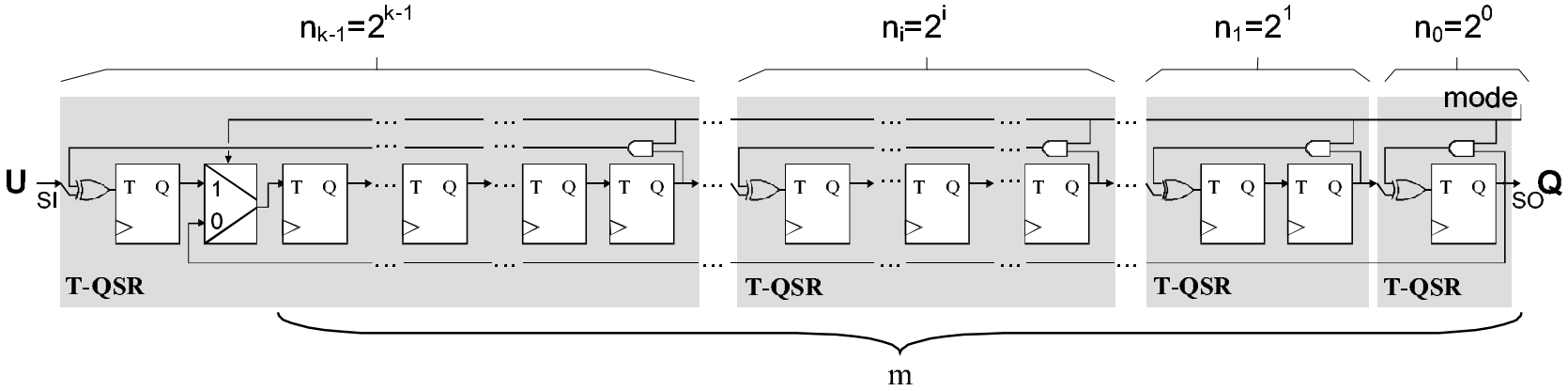
Existing solutions for seeding of m-bit T-FSR







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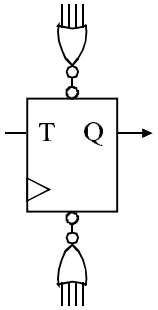
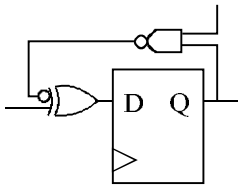
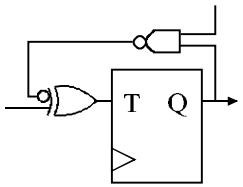
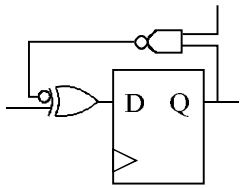
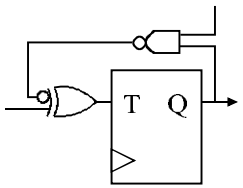
Comparison of maximal frequency of presented solutions

AMS Std. Cell Library, 0.8um Double-Metal CMOS 5V, C_{load}=0.5pF

			
TPG mode	370 [MHz]	345 [MHz]	347 [MHz]
			
scan mode		373 [MHz]	323 [MHz]

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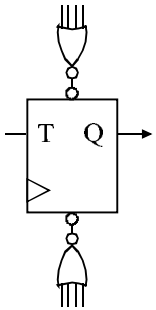
Comparison of area overhead of presented solutions for n-bit T-FSR

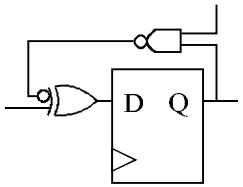
AMS Std. Cell Library, 0.8um Double-Metal CMOS 5V, C_{load}=0.5pF

T-FF 2232 [μm^2], D-FF 1860 [μm^2],

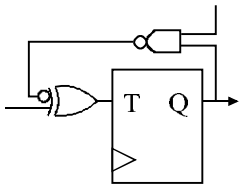
IOR 1302 [μm^2], NAND 558 [μm^2], IOR+NAND 1860[μm^2]



m*2790 [μm^2]



m*3720 [μm^2]



(m+1)*2232+ $\log_2$(m)*1860 [μm^2]

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Conclusions

Properties of T-FSR equipped with quasi-scan mode

- Similar timing properties like existing solutions
- Lower area overhead
- Can be easily integrated to the scan path
- Can be easily tested by single serial pattern