Bridging the Testing Speed Gap: Design for Delay Testability

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Abstract

The economic testing of high-speed digital ICs is becoming increasingly problematic. Even advanced, expensive testers are not always capable of testing these ICs because of their high-speed limitations. This paper focuses on a Design for Delay Testability technique such that high-speed ICs can be tested using inexpensive, low-speed ATE. Also extensions for possible full BIST of delay faults will be addressed.

1 Introduction

The speed of digital integrated circuits has increased tremendously in the past years under the push of demanding system applications. Currently, clock frequencies around 1 GHz are no exception [1]. When lowering the operational temperature of devices, using the existing processing capabilities, even higher clock frequencies can be obtained [2]. Unfortunately, the testing and related costs of these advanced ICs are identified as one of the most critical problems for future development [1]. Although the speed and accuracies of ATE has improved over the years, it is difficult to keep up with the advances in silicon [3]. Even if this could be achieved technically, the resulting costs would be enormous. It is predicted that the cost of testing a chip will exceed its processing cost in the future [1]. The clock frequency of the IC plays a major role in the calculation of the overall test cost. With the increase in (speed) performance, the costs are expected to multiply by four in the future. These costs can be decreased if the chip is tested at a significantly lower speed than its operating speed while still guaranteeing its high-speed behaviour. This paper uses a new DfT technique where this can be achieved. Current BIST techniques are inadequate to test high-performance devices. This is mainly due to the fact that the BIST is usually conducted at low frequencies. In section 5, based on the previous DfT technique, a BIST approach will be presented which operates at low clock frequencies to detect the delay faults otherwise only detectable at high clock frequencies.

2 Delay-Fault Testing based on Clock Control

The rapid increase in clock frequencies of digital circuits due to deep sub-micron technology have created an increased concern about (cost-) effective detection of delay faults. In reference [4] it has been shown that timing faults can become dominant over conventional faults in some cases. Unfortunately, these faults will not influence the steady-state logic functionality of an IC. It is therefore not possible to detect these faults by slow speed stuck-at testing methods. Current BIST approaches and (non at-speed) functional tests will also not solve this problem. One basic approach to tackle this is employing correlation-based testing methods not requiring high-speed test equipment. There is, for instance, a technique that uses the relation between (low-speed) I_{ddq} measurements and the maximum operating frequency of circuits [5]. Another method is based on the relation between the power-supply voltage and propagation-delay times in circuits [6]. These correlation-based approaches have a limited level of confidence, which is not always acceptable in high-quality products. The other basic (direct) approach is based on the introduction of special Design for Test (DfT) structures [7,8]. In some publications, clock signals of latches or flip-flops are manipulated or additional test signals introduced resulting in the transformation to lower timing requirements for the testers [9-11].

A pioneering paper on the latter subject has been written by Agrawal et al. [9]. They proposed a pulse-triggered flip-flop with two operational modes. Basically, a dynamic latch was introduced inside a traditional master-slave flip-flop. The resulting three latches circuit allowed modulation of flip-flop delay with a changing clock-pulse width. In a digital circuit, all signal paths must satisfy the timing relationship that the clock-time period has to be larger or worst-case equal to the propagation delay time of a flip-flop, its set-up time and the delay between flip-

flops. This delay can result from combinational logic or interconnection-line parasitics. The above-mentioned three latch construction has a normal and a test mode. In test mode, increased pulse width of the clock increases the propagation delay of the flip-flop. Assuming that the set-up time and delay in combinational logic/interconnect remain unchanged, the clock period must become larger. Hence, a slower clock frequency is able to test critical or other paths with the same timing specifications. One of the most significant implementation issues in a pulse-triggered flip-flop is realization and propagation of precise pulse width at the chip level. A small pulse width needed for high-speed normal mode operation may appear significantly distorted due to interconnect impedance. The next section provides a better alternative.

3 The Controlled Delay Scan Flip-Flop

A flip-flop delay can be also be *controlled* by an *additional* test-mode clock. These flip-flops are called controlled delay flip-flops (CDFFs) [10,11]. A CDFF differs significantly in concept and in implementation details from the pulse-triggered flip-flop. These differences are crucial. In the references [10,11], several types of flip-flops have been introduced each at all primary inputs and outputs of a combinational logic IC to detect possible delay faults in the combinational logic part. The faults and required conditions for the test signals (clock and test clock) have been generated using a delay-fault test-pattern generator. In *this* paper, the detection of possible delay faults in busses between embedded sequential blocks are presented as shown in Figure 1. This type of architecture often occurs in high-speed digital video processors and microprocessors [12].

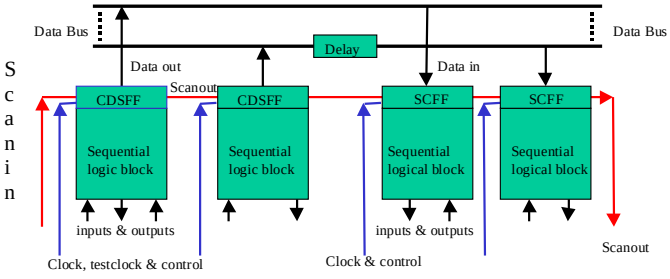

Figure 1: *Detecting an (interconnection) delay fault in a bus using the CDSFF concept. SCFFs are scan FFs.*

Furthermore, delay faults in interconnection lines ("delay" in Figure 1) represent a realistic situation as these are expected to dominate the speed behaviour in future deep sub-micron systems. As scan testing is often used for stuck-at testing in ICs anyhow, we have developed a Controlled Delay Scan Flip-Flop (CDSFF) based on a conventional scan flip-flop (SCFF). This has the additional advantage that also the delay between embedded blocks can be detected and shifted out in a serial, scan-like manner. The CDSFF allows master to slave data transfer on the rising edge of the test clock. In the test mode, the propagation delay τp of the flip-flop is controlled with the test clock Tclk. A schematic diagram of the CDSFF is depicted in Figure 2. The scan-input Sci and scan output Sco become active with the signal labelled "Mode". Di_1 and Do_1 are the respective data input and output while Clk denotes the regular clock.

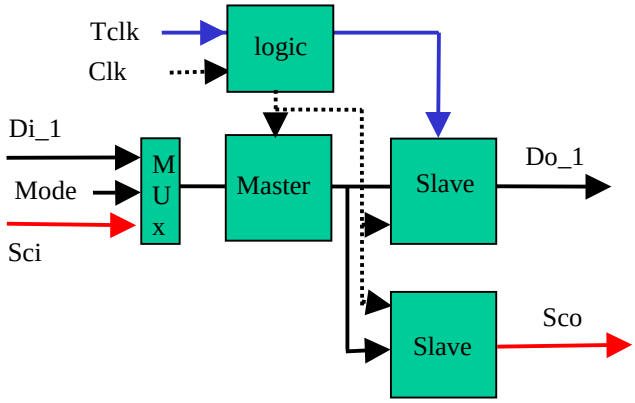

Figure 2: *Block diagram of the Controlled Delay Scan Flip Flop (CDSFF).*

The significance of the additional test clock is illustrated in Figure 3. This figure depicts the test mode timing diagrams of detecting an interconnection delay-fault labelled "del" with CDSFFs.

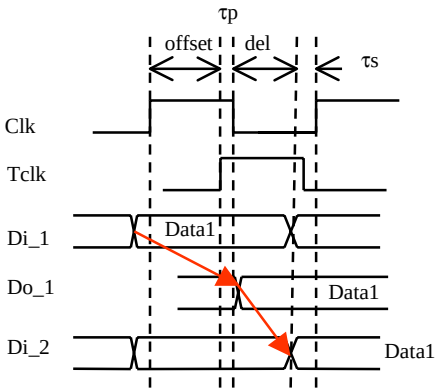

Figure 3: *Timing diagram of the CDSFF in test mode and assuming a 50% duty cycle of clock and test clock.*

In the normal mode, the test clock has no function and is held high ensuring normal (scan) flip-flop operation. However, during the *testing* of the IC, it operates as a clock with tester programmed time offset ("offset, Figure 3) with the regular clock Clk. The test clock goes to a pre-determined sub-set of CDSFFs in the IC

(Figure 1). When the test clock is active, it controls the data transfer from the master to the (top) slave latch (Figure 2) in the DCSFF. In other words, depending on the timing relationship between the clock and test clock, a delay is introduced between master and top slave latch of the CDSFF (Figure 3). The net effect is that the CDSFF data "Data1" appears at its output Do_1 after the additional delay at the rising edge of Tclk and internal propagation-delay τp. After the delay of the interconnection line ("del") it arrives at the input Di_2 of the receiving regular scan flipflop (SCFF). Before the set-up time τs of the SCFF, the data can be read in the master part of the SCFF. The test mode clock period should be sufficiently large to accommodate the delay time in the interconnect lines. It is obvious that as the offset is increased, the period of the clock is also increased or the clock frequency is reduced. In other words, the clock frequency can be reduced while the combinational circuit delays are tested with the same delay margins. The realisation of the CDSFF requires additional transistors and an additional test mode clock input as compared to a normal scan flip-flop as indicated in Figure 2. Depending on the number of CDSFFs needed, a set of test clock buffers and interconnects may be required. The choice where to introduce CDSFFs is guided (and limited) by critical delay path analysis. The cost of implementation is high but this is compensated by cheaper, slower test systems.

4 The CDSFF behaviour and its use in a system environment

Two transmission gate pairs (TGs) are incorporated in the implementation of the CDSFF. They are part of the block labelled "logic". The first TG is added between master and (top) slave latch while the second one is added in the feedback path of the (top) slave. Both TGs are controlled by the test clock. Addition of the first TG is obvious as it controls the master to slave data transfer. The need for second TG is to keep the data output always in a driven mode. The CDSFF has been simulated in HSPICE using the technology data of the 0.35µm TSMC CMOS process. An upgraded version of 0.25µm is currently under investigation. The results are shown in Figure 4. For simplicity, Clk and Tclk have a 50% duty cycle in Figure 3. As only the time delay between the rising edges of both is of importance, similar results can be obtained by changing their duty cycles and frequency simultaneously. If "Mode" is low, the CDSFF acts as controlled-delay element. At the rising edge of Clk, the input data Di_1 is read in. At the rising edge of Tclk it becomes available at the output Do_1. If "Mode" is high, the CDSFF acts as a regular (scan) flip-flop.

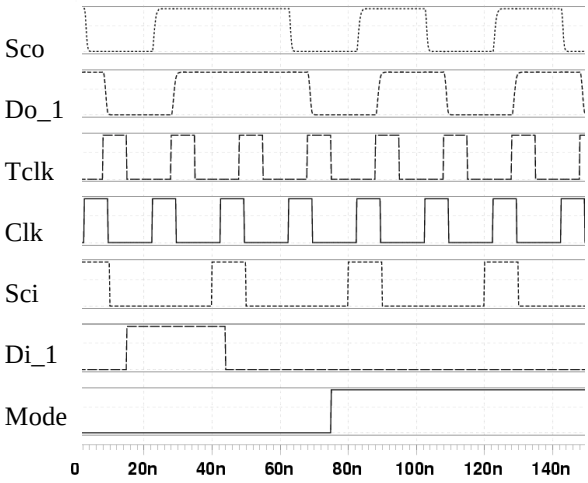

Figure 4: *Simulated circuit behaviour of the CDSFF in HSPICE based on 0.35µm TSMC technology [20].*

The scan input data Sci becomes available at the scan output Sco at the rising edge of Clk. Tclk plays no role. In order to illustrate the concept at system level (Figure 1), two simulations were carried out. One assuming no delay fault in the interconnect line (Figure 5, Sco_g), and the other in the case of a delay fault (Figure 5, Sco_f).

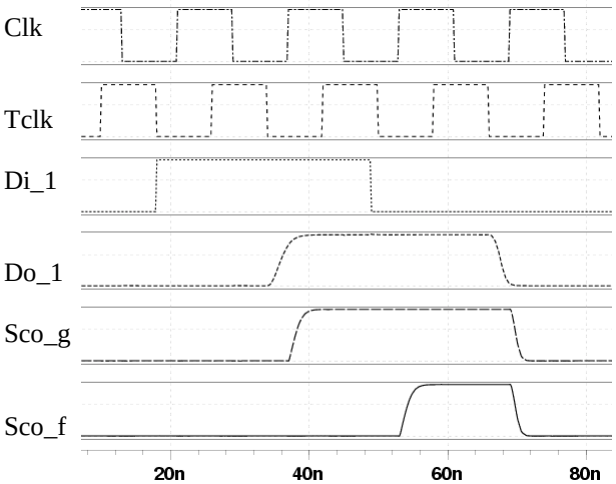

Figure 5: *Simulation results of the CDSFF in a system environment. Fault-free behaviour (Sco_g) and faulty (Sco_f) behaviour under influence of an inter-connection delay fault.*

The duty cycles used for Clk and Tclk are 50% and the frequency is 60MHz. The figures show the correct detection of the delay fault. It is remarked that the clock frequency can be much lower in the case the duty-cycles of Clk and Tclk are changed. This is further elaborated in section 5.

5 A BIST Environment for Detecting Delay Faults

5.1 Introduction

In the past, several papers have been published with regard to BIST for detecting delay faults [13-19]. Most efforts have been confined to generating the required two-pattern tests for detecting delay faults. The "*adjacent testing*" approach uses test pairs which only differ at a single position. As a result, only simple hardware is required [14]. A more sophisticated technique starts with a predetermined set of test pairs, e.g. from ATPG, like in our case. Here, hardware is designed which generates sequences in which the test pairs (initialisation and propagation vector) are embedded [15]. The key elements in these generators are special Linear Feedback Shift Registers (LFSR) [16] or Multiple Input Signature Registers (MISR) [17]. Although rarely discussed, the evaluation of the responses can be carried out in a similar way as in "conventional" digital BIST approaches using signature analysers. A completely different approach makes use of controlled oscillation of the block involved [18]. However, the problem is measuring the high oscillation frequency either internally or externally. In our approach, additional hardware has been designed to carry out the BIST at low clock speeds [10, 11]. There is an option to include the above mentioned (partial deterministic) two-pattern generation and evaluation by means of MISRs (*Full BIST*) or choose for external application and evaluation by means of slow-speed (< 50MHz) ATE. This section is focussed on the last option.

5.2 Global set-up of the low-speed BIST

In figure 6, the set-up of the suggested BIST architecture is shown. Beside the full-BIST option employing MISRs for two-pattern generation and response evaluation, the key elements in the low-speed approach are the Programmable Delay Lines (PDL) and Duty-Cycle Control (DCC) blocks. As example, the test described in [10] has been used.

Figure 6 shows a number of blocks which are of crucial importance, besides a number of registers and control logic. Subsequently, the programmable delay line (PDL) and the duty-cycle control (DCC) blocks will be discussed in more detail.

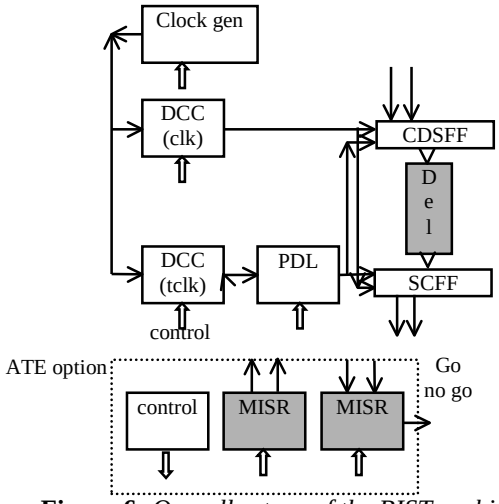

Figure 6: *Overall set-up of the BIST architecture.*

5.3 The design of the different BIST parts

5.3.1 The Programmable Delay-Line (PDL)

The most crucial part of the BIST circuitry is the programmable delay line. There are several ways of implementing this structure, e.g. such as discussed in [19]. In our case inverter chains were used, tapped at uneven locations by means of NANDs (Figure 7). The transmission gates have been inserted for security reasons with regard to the OR-wired (buffered) output line. The decoder with addresses A0…A6 is a standard implementation of a 7-line-to-127-line decoder using NANDs.

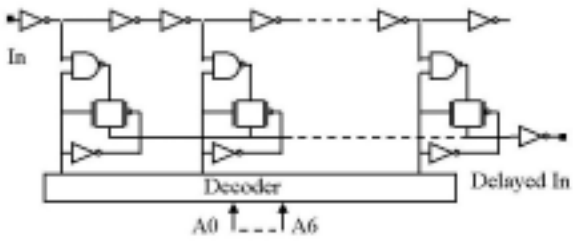

Figure 7: *Design of the programmable delay line.*

A HSPICE circuit simulation was carried out to verify the behaviour of the circuit. The minimal timing resolution of the design was set to around 500ps. The maximum obtainable delay between the input and output becomes in this case 63.5 ns. Figure 8 shows the low-speed case (20 MHz) with a programmed delay of 12.5 ns. Also in the high-speed case (130 MHz) with very little delay (500ps) the circuit worked satisfactory.

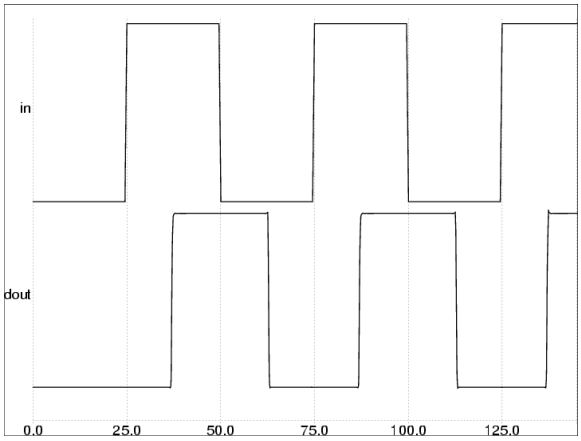

Figure 8: *HSPICE circuit simulation of the PDL in the low-speed mode (20 MHz). Time axis is in ns.*

5.3.2 Programmable Duty-Cycle Control (DCC)

The second important component in the BIST architecture is the duty-cycle control (DCC) block. There are two DCC blocks required in the BIST architecture: one for the clock and one for the test clock. The simplest implementation consists of the previously discussed programmable delay line in combination with a logic block as shown in Figure 9.

The frequency range is between 10 and 50MHz, and the duty cycle can be varied between 5% and 95% with minimum pulse duration of 500 ps. It requires 8 bits (A0 up to A7) to control this duty cycle. A HSPICE circuit simulation of this block for the low speed mode (20 MHz) and a duty cycles of 8% and 95% is shown in Figure 10. These values are also used in the overall BIST simulation in the Figures 11 and 12. Conventional stuck-at testing can test the PDL and DCC circuits.

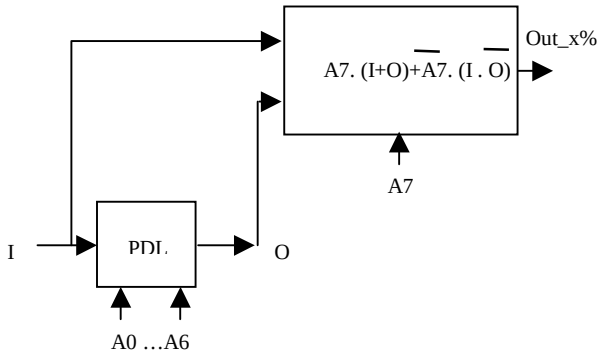

Figure 9: *Design of the programmable duty-cycle control (DCC) block, using the programmable delay line (PDL).*

It is clear from above that the PDL is the most complex part of the BIST structure *due to the required delay and duty-cycle resolution.* However, in practice some of the PDL parts can be combined. For the sake of simplicity this has not been implemented here.

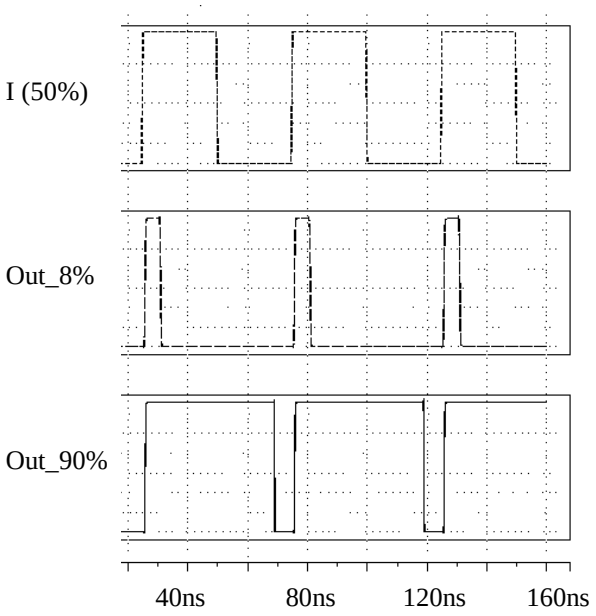

Figure 10*: Circuit simulation of DCC in low-speed mode (20MHz). Input signal duty-cycle is 50%, and outputs have 8% and 90% duty-cycle respectively.*

5.4 Experimental Results

The previously described parts have been combined into the BIST architecture as depicted in Figure 6. For the sake of simplicity and insight of the structure, the control parts and MISRs for signal generation and evaluation have been omitted in the simulations in Figures 11 and 12. Figure 11 shows the low-speed BIST in the fault-free case. The critical path has a delay of 4750 ps.

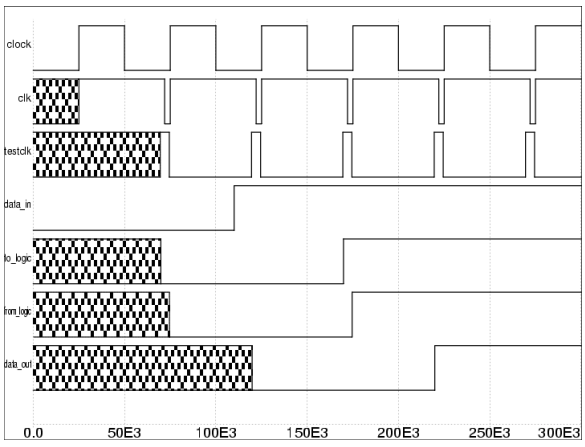

Figure 11: *Simulation of the BIST architecture in the low-speed , fault-free behaviour. Delay:4750 ps.*

Next, in Figure 12, the low-speed operation is simulated with values determined from simulations for the required frequency, duty-cycles and delay. For this delay fault, the frequencies are 20 MHz, duty cycles of clock and test clock 95.8% and 10.8% respectively, and a delay of 45 ns between clock and test clock. As can be seen from the simulations, the delay fault is detected in the last case. The simulations show that the concept of low-speed BIST works. Monte Carlo simulations have been carried out to determine the changes in the PDL and DCC delay times as function of Vth, tox, W/L (10%) and Vdd (5%) variations. The maximum W/L variation dominates the maximum change in delay time (~ 6% for 45 delay stages).

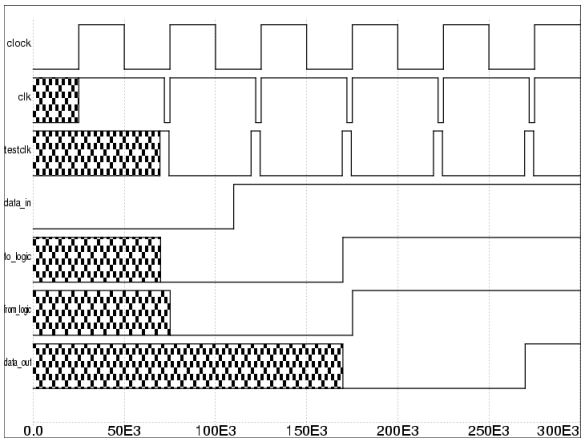

Figure 12: *Simulation of the BIST structure in low-speed mode (20MHz) detecting the delay fault. Delay:5350 ps.*

6 Conclusions

A Controlled Delay Scan Flip-Flop (CDSFF) and associated BIST architecture has been proposed for detecting small delay faults in digital high-speed circuits. The method avoids the requirement of an expensive high-speed tester. Depending on the application, a full BIST or a CDSFF approach employing a low-speed tester can be used. The DfT hardware and associated BIST architecture is based on different concepts as compared to previous approaches. The manipulation of delay between and duty cycles of the clock and an additional test clock as well as the use of new controlled delay scan flip-flops are crucial in this respect. Simulations of the DfT parts, as well as the overall BIST architecture indicate the feasibility of our methods.

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