Using on-chip Test Pattern Compression for Full Scan SoC Designs

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In todays mixed signal System-on-Chip designs advanced Design-for-Test techniques become more and more important to meet test coverage and quality requirements. However, standard strategies often cannot be used because of design specific requirements like the limitation of available input and output pins.
This paper describes the Design-for-Test strategy of the latest version of Motorola's chip family for a mixed signal application. Deterministic test pattern, which are generated using an ATPG tool, have been used to stimulate the design and achieve efficient and high test coverage. The memories are tested by using a memory BIST implementation. The limitation of available digital input and output pins is solved in two ways. Analog input pins have been modified to serve as digital pins in test mode. On-chip test pattern compression using a multiple input shift register (MISR) is used to reduce the number of required output pins. Failure diagnostic capabilities have been implemented to allow debug of failing devices. The paper describes the test strategy for the System-on-Chip device and outlines the design flow which was used to implement it.

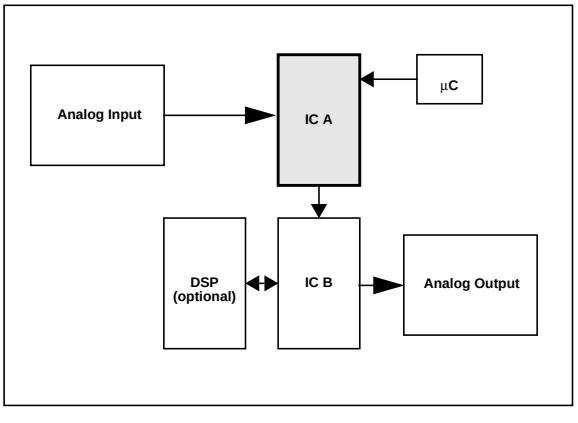

Figure 1: Application Chip Set

Overview of the Design and Application

Figure 1 shows the basic structure of the application. The chip set consists of two application specific mixed signal integrated circuits (IC A and IC B), which do have the capability, to interact with a micro controller or an optional DSP core.

IC A is the frontend circuit, which contains the analog interfaces for the application. Having 40% of the design being analog circuitry, the number of available digital ports is very limitied. A new DFT methodology is required to achieve a fault coverage of more than 95%. The digital part of the design itself consists of a core, embedded memories and application specific components. The percentage of digital circuitry in the second application specific IC is much higher, therefore standard DFT methods can be used.
The silicon is manufactured in a high performance dual poly 0.25µm CMOS process technology. The Power Supply Voltage is 3.3 V.

Design-for-Test Strategy Overview

The predecessor of the current chip set is tested using test pattern which are derived from application specific simulation runs. Basic stuck-at fault coverage for the digital part of the design is achieved by applying functional test pattern without any structural test method.

For the new chip set an enhanced test strategy is required to improve test coverage and failure analysis. The selection of any standard methodology like full or partial scan is constrained by only having a single digital output pin available. The design also misses the required amount

of digital input pins for a full scan design. Thus, a new test strategy has to be defined which covers all of the digital part of the analog mixed signal design. However, to achieve a stuck-at test coverage of more than 95% a structural test strategy which allows the usage of Automatic Test Pattern Generation tools must be used. Logic Built-in Self-Test is found not to be an adequate solution because of required test coverage.

A new strategy is developed which is outlined below.

- Full scan test strategy is implemented on all digital blocks of the design.
- All scan chains (preferably balanced), are connected to scan input pins.
- All outputs of the chains are fed into a Multiple Input Shift Register (MISR) which provides on-chip test pattern compression.

A Multiplexer allows to connect the output of the MISR or the output of a scan chain to the scan-out pin.

An overview of the Design-for-Test architecture is shown below:

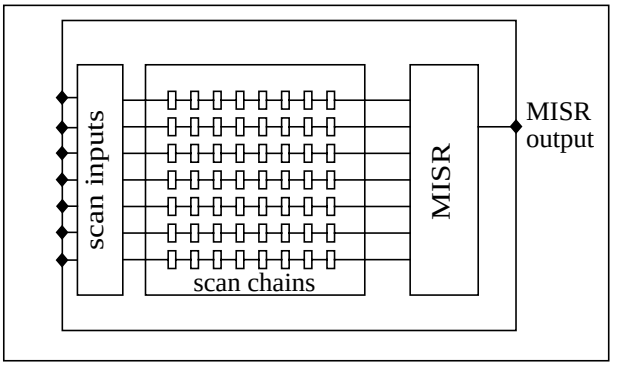

Figure 1:Design-for-Test Architecture Overview

The main advantage of this Design-for-Test strategy is, that only a single digital output pin is required to test the digital parts of the design. No loss in test coverage must be obtained. If additional observe points are added to the design, which make the “pseudo full scan design” to a full scan design, an ATPG tool can be used for test pattern generation. Though these generated test pattern cannot be used on the tester, as the additional observe points are not available on the tester, they can be used to stimulate the design during simulation. Simulation results can be used to prepare test pattern. (Please see the paragraph about the Implementation Flow later on).

The number of available input pins during scan test mode is increased by modifying analog input pins to allow their use as scan input pins. The required modifications to the analog pins are described later in this paper.

The test strategy for the digital blocks is complemented by the following items:

- Built-in Self-Test is implemented for embedded memories which are not connected to the external bus.
- Functional memory testing is used for embedded memories which are connected to the external bus.
- All modules can be switched off (power-down) to allow IDDQ measurements.
- Analog modules are tested by functional tests developed on the tester.

Analog Input Pin Modification

To increase the number of available input pins analog pad cells must be modified. The purpose of the new pad cell is to use analog I/O’s as scan inputs during scan test mode.

This is achieved by the following modification:

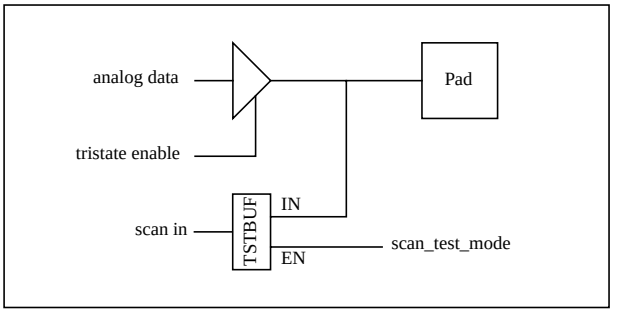

Figure 2:Analog Pad Cell used as scan input

An additional buffer (TSTBUF) is connected to the analog I/O cell. This buffer is placed in an analog power domain and preferably is placed adjacent to the analog I/O padcell concerned (see Figure 2). An input protection network is provided to the input (IN) of the buffer which consists of a series resistor (solicited poly resistor) and of secondary ESD protection diodes. Therefore input IN is connected to the analog I/O padcell. The input IN can be enabled/ disabled using the input EN. This input of the buffer is connected to the device input which controls whether the device is in scan test mode or in normal functional mode. Thus, the influence of the additional connection of the analog input pin to the digital part of the device can be minimized during functional mode.

On-chip Test Pattern Compression

Since there are a limited amount of device pins and there are many flip-flops in the design, an approach is needed to reduce the number of test pins while reducing the depth of the scan chains. On-chip test pattern compression is required because only a single digital output pin is available for testing the digital part of the device. As more than 20 scan chains are inserted in the various digital blocks of the design, test results have to be compressed into single bit information. An on-chip multiple input shift register (MISR) is used to perform this task. Since the MISR produces a single scan output, the rest of the chip pins can be used to drive the input of all the scan chains.

The MISR is implemented as a Type 2 (internal XOR) using a primary polynomial. The MISR is 31-bits wide, and each scan output signal bit feeds into a bit position of the MISR register. Rather than generating a signature, the MISR will be used to combine all the scan chain outputs into one signal. A MISR was chosen rather than an XOR tree to reduce the probability of a fault masking between the chains. A single bit of the MISR is brought out to the device using a digital output pin. This output is strobed during scan test mode continuously to avoid aliasing.

Failure Analysis Capabilities

The usage of the on-chip MISR drastically reduces any failure analysis capabilities which are accompanied by using a structural test approach like full scan design.

This reduction is not acceptable for the device. Although, there is the restriction of only having a single digital output pin, it still needs to be possible to directly investigate the content of each flip-flop of the design.

For this purpose an additional module is implemented to multiplex a particular scan chain or the MISR combination of all the scan chains into a single signal that can be routed to the device output. The architecture of the module is shown in Figure 3. A 32:1 multiplexer is used to select a particular scan chain of the chip or the MISR combination of all the scan chains. The output of this multiplexer drives the output, which can be connected to the chip scan output pin. The 31-bit MISR is used to compress all the scan chains into a single signal, which is selected when the scan control registers are all zeros. Scan chain outputs connected to the multiplexer input signals are selected in order with the scan control signal values greater than zero. For example scan_out[0] is selected if the scan control value of ‘00001’ and scan_out[30] is selected if the scan control value is ‘11111’.

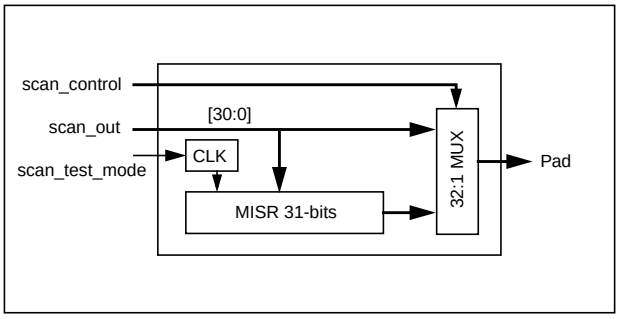

Figure 3:Pattern compression and failure analysis architecture

The scan output signal of one scan chain is used as scan input signal of the following scan chain. This feature is used to enhance debug capabilities, to get similar debug capabilities as in a full scan design.

It is key that the registers, which are controlling the different failure analysis modes, are not part of any scan chain. They have to be set to a defined value in the setup procedure of the scan test using the external bus of the device and have to retain this value until the test is finished.

The additional logic, which is introduced by the failure analysis capabilities is not fully covered by the ATPG pattern. Functional test pattern have to be developed and fault simulated for these parts of the design.

Details of the on-chip pattern compression and failure analysis implementation of the device are shown in Figure 3.

Design-for-Test Implementation Flow

The Design-for-Test strategy requires additional steps in the implementation flow compared to a standard design flow for full scan design. The different steps are shown in Figure 4 and outlined in this paragraph.

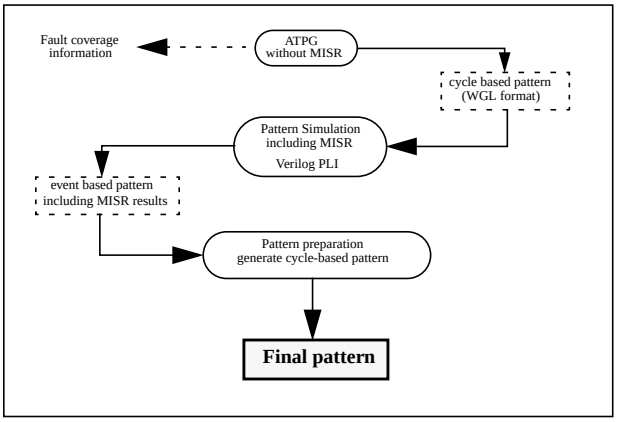

Figure 4:Implementation Flow

Test synthesis of the testability structures is performed using Synopsys Design Compiler and Design Compiler Plus synthesis tools. The Multiple Input Shift Register (MISR) and the memory BIST implementation is described in Verilog RTL code. Test points to fix Design-for-Test design rule violations, like not transparent latches during scan test mode, read/write stability of embedded RAM memories during shift mode, disabling of clock gating during shift mode, are also included in the RTL code. The automatic test point insertion by Synopsys DC Expert Plus is not used.

It is key for the overall test strategy that there are no sources for Logic X simulation values in the design. Logic X values in simulation would make the MISR result unpredictable and on-chip test pattern compression would not be usable. Therefore, all flipflops must be resetable. All on-chip tristate logic, like internal tristate busses, from previous designs of the chip set family were removed or converted to a multiplexed bus approach.

Synopsys DC Expert Plus is used for scan chain insertion on top level of the design. Initially the design is compiled “test-ready”, which means that scanable flipflops are already inserted in the design replacing normal flipflop functionality, but no scan routing is performed yet. DC Expert plus generates balanced scan chains of equal length to minimize overall scan chain length.

For automatic test pattern generation the Mentor Graphics’ ATPG tool Fastscan is used. Fastscan supports automatic test pattern generation for full scan designs. As a full scan design technique implies scan input and scan output signals for every scan chain, additional user defined output pins have to be added to the device in Fastscan. These “virtual” output pins are used as scan outputs during ATPG.

As the Multiple Input Shift Register is not part of any scan chain, the ATPG tool treats these sequential elements as black boxes and converts them into tied-to-X gates. This fact has got two major implications: First the MISR itself and the fanout of the MISR is not testable by the ATPG tool. All injected faults of the related gates are ATPG untestable and therefore lower the test coverage statistics. Second, the MISR output value will be always masked in the test pattern generated by the ATPG tool. Therefore, the test patterns, which also reference the virtual output pins for the scan chains can not directly be converted into ATE format. The test pattern generated by the ATPG tool can only be used as simulation stimuli.

The analog blocks of the design are modeled in Fastscan as black boxes. As this could lower the achievable test coverage quite significantly. The interfaces between analog and digital parts must be defined. Ideally first gates within the digital blocks interfacing to the analog parts are flipflops, which are part of scan chains.

ATPG patterns are generated in WGL format. This format is the standard format used within Motorola’s SoC Design System Stingray. The design system provides simulator extensions using the Verilog Programming Language Interface (PLI) which allow to apply test pattern in WGL format to the design during simulation. This is normally used to verify the correctness of the test pattern during timing simulation using a Verilog HDL simulator. Simulation results are compared with expected results in the WGL test pattern. Any mismatches during resimulation will be highlighted.

As already mentioned, in that special case, the WGL test pattern contains data that cannot be used for testing the device because the file contains virtual scan outputs and the MISR output is masked. The PLIs can be used, to stimulate the device and to generate meaningful simulation results, which also contain the MISR output. For functional timing simulation on gate level the Verilog simulator Verilog-XL of Cadence is used.

The simulation output data is generated in event based Verilog Change Dump (VCD) format. This event based format is converted to a cycle based tester format. Test Development Series software of Fluence (formerly TSSI) is used for this design step. Motorola’s SoC design system provides a highly automated flow.

The resulting WGL test pattern file is verified again using

the WGL PLIs during functional simulation. Additionally the fault simulation is performed using Cadence Verifault Fault Simulator to calculate the test coverage of the test pattern for those faults which can not be tested by the ATPG tool (e.g. the MISR gates, which are categorized as ATPG untestable during the ATPG process). Both resimulation and fault simulation is performed including backannotation of timing data from place and route (parasitic information) to achieve timing accurate simulation results.

In the final step the test pattern in WGL format are translated into tester specific data. Additional test program data is derived from the design database to provide all data required for the full test program. The Teradyne A580 mixed signal tester is used to test the device.

Design-for-Test Implementation Problems

Main problems which have not been foreseen up front are all related to logic X propagation to the Multiple Input Shift Register. The Mentor Graphics DFT tool suite supports logic Built-in Self-Test implementation. In this flow X propagation is checked during automatic test pattern generation by various DFT rules. As the device does not use a standard BIST methodology the built-in DFT rules could not be used during Fastscan ATPG. The first time X propagation is identified in the design flow, is during test pattern resimulation and investigation of simulation results. This implied a significant iteration loop to correctly setup the ATPG tool by changing the test setup routine or modifying the design. Normal test pattern generated by an ATPG tool include a significant number of “don’t care” and mask values. Such values can not be handled by a MISR. Simulation has to provide the exact logic value.

Logic X sources in the design are especially related to embedded RAMs and analog blocks. Other X sources had been solved up front. The initial test setup routine did not include a procedure to put the embedded RAMs in a defined state. This would not be a problem for normal ATPG. For the on-chip test pattern compression it is a major problem as RAM outputs will be logic X. These logic X values will be captured by sequential elements, which are part of a scan chain during the capture cycle of the scan test and will be propagated into the MISR during scan shifting. The test setup of ATPG, which already contained a reset sequence, must be enhanced to load the contents of all embedded RAMS into a defined value.

Analog modules must be modified to output a defined, not tristate, logic value, if the device is in scan test mode. As this was not included in all analog module specifications additional logic gates are introduced, which tie the interface signals between analog and digital portions of the design to a known state. These fixes are performed in the RTL code. No automatic test point insertion was used.

Memory BIST implementation

The System-on-Chip design contains several small memories that needed to be tested. Memory BIST was required since some of the ROMs where hidden from the external serial bus interface. BIST logic for each memory was deemed to be too much overhead due to the size of the memories. Therefore a minimal global memory BIST concept was designed to achieve a good memory fault coverage.

Since all RAMs in the design were accessible from the external serial bus interface, BIST writing to the memories were accomplished over this bus, using the tester as a BIST writer. Using the tester as the BIST writer provides the maximum flexibility in the BIST algorithm at the expense of test time writing the memories over the serial interface. This reduction in test time was of minor issue since the test time is dominated by analog test time.

In addition to the BIST mode control register, each memory in the design is driven by an incrementing BIST address register, which is used to sequentially read each memory location of each memory concurrently. The output of the memory read access is then fed into a MISR which produces a compressed 1-bit output signal that is treated in the same way as an internal scan chain output. The overhead of the MISR can be reduced by converting a data register used in normal operation into a MISR. This new MISR behaves as a data register during normal operation, but implements the MISR functionality in the BIST read mode. In addition, a MISR could be shared for several local memories by pre-XORing memory outputs and feeding this new XORed value to the input of the MISR.

The BIST address counter is reset only when the input reset pin is asserted. The value is incremented after each read operation, and is allowed to rap-over when the maximum value is reached. Memories that do not have 2^n memory spaces are disabled during invalid address, so that unknown values are not propagated to the MISR hardware.

Results

Table 1 shows a statistic of the design and the results,

which are achieved by using the described Design-for-Test methodologies.

Number of digital signal pins (all / in / out) in scan test mode	30/29/1
Number of flipflops	7735
Number of scan chains	23
Max number of flipflops per scan chain	380
Initial stuck-at fault coverage	92%
Enhanced stuck-at fault coverage	96%
Combinational pattern only coverage	83%
Additional sequential pattern coverage	13%
Total number of scan pattern / loads	1200
Number of combinational pattern / loads	1000
Number of sequential pattern / loads	200
Total number of test vectors for scan	~600 000

Table 1

As shown in Table 1, the original test pattern set could not fully achieve the goal of a test coverage higher than 95%.

The ATPG tool was not able to efficiently create test pattern for testing logic which surrounds embedded RAMs within the design. Though RAM Sequential algorithms have been used during ATPG, a lot of faults are declared as ATPG untestable because of limited capabilities of the ATPG tool to modify the address range when testing logic surrounding RAMs. To workaround this limitation RAMs are modeled as registers with a single address only and sequential algorithms of the ATPG tool are used. The test coverage improved by 4% when using this approach.

Additional fault coverage is achieved by applying IDDq test vectors to the device. This IDDq vectors complement to stuck-at fault coverage. IDDq vectors are identified using Synopsys PowerFault IDDq tools.

Conclusion

A new Design-for-Test strategy has been developed successfully for the first SoC device of a new Motorola chip set. This strategy combined the advantages of automatic test pattern generation of high test coverage and efficient test pattern generation with the advantages of on-chip test pattern compression resulting in a methodology for low pin count SoC devices.

Future SoC devices will use the same or similar strategies. Improvements will be made on following designs regarding the initialization and reset sequence for registers and embedded RAMs. Also the Memory Built-in Self-Test for the embedded RAMs will be enhanced toimprove the test coverage further.