

Comparison of Defect Detection Capabilities of Current-based and Voltage-based Test Methods.

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Abstract

The industrial default to test random logic is based on stuck-at fault test patterns applied via scan-chains. This test-method can be described as static voltage testing. A second well-known method is I_{DDQ} testing, which can be described as static current testing. This second method is especially suited for detecting resistive shorts. For deep sub-micron technologies new defect mechanisms start to become important. Especially, opens are a much-feared type of defect since static test methods are less suited to detect these defects. Dynamic test methods such as delay-fault testing and transient current testing could fill this gap in the test suite. The paper gives an overview of the aforementioned test-methods including some of the new current-based test methods necessary for deep sub-micron technologies and their defect detection capabilities.

1 Introduction

ICs contain millions of transistors nowadays. Each of these transistors can be faulty owing to manufacturing defects or problems during the handling or packaging. To assure the quality levels expected by the customers, it is necessary to test each single chip. The most common method to test random logic is by applying, via scan-chains, test patterns, which are based on the (single) stuck-at fault (SAF) model. Generally the patterns are applied at a speed well below the operational speed of the device and the method can be described as *static voltage-based testing*. The widespread use of the method is based on the ease to generate test patterns. No knowledge of the function or the layout of a circuit is necessary and automated test pattern generators are used to generate the test input stimuli and the expected output responses.

Although the stuck-at fault model is the *de facto* metric for testing it is also well known that the single stuck-at fault model is not a very realistic description of real defects [1][2]. The test quality (e.g. the number of bad devices that pass as good) strongly depends on the fortuitous detection of non-targeted faults. This quality level is usually expressed in a parts per million (PPM) figure, which denotes the number of faulty devices per mil-

lion devices shipped as good. Improvements in the quality level can be expected by using more accurate fault models in combination with other test methods. This was well recognised over a decade ago when quiescent current testing (I_{DDQ}) was introduced.

In an I_{DDQ} test one observes the (leakage) current of the power supply when no clock activity is present (*static current-based testing*). In CMOS technologies the leakage current used to be very low and an elevated current indicated the presence of defects. I_{DDQ} tests are by far superior in detecting resistive shorts [3] compared to static voltage-based testing. Beside resistive shorts current-based tests are also capable of detecting a wide range of other defects such as gate-oxide shorts [4] and stuck-opens [5]. Furthermore I_{DDQ} testing is capable of catching defects, which do not cause logic faults but nevertheless make the device unacceptable for the customer or form a reliability risk, as for example excessive power consumption owing to shorts between V_{DD} and V_{SS} .

Until now the combination of static voltage testing and static current testing was sufficient to realise the quality levels required by the customers. However for deep sub-micron technologies new defect mechanisms start to become important. Especially, opens are a much-feared type of defect since static test methods are less suited to detect these defects. Dynamic test methods such as delay-fault testing and transient current testing could fill this gap in the test suite.

With the inclusion of the dynamic test methods we can now distinguish four classes of test methods:

- Static voltage-based tests (e.g. SAF based test patterns applied via scan chains).
- Dynamic voltage-based tests, such as delay-fault testing, “at-speed” testing, and functional testing.
- Static current-based tests, such as the conventional I_{DDQ} testing but also ΔI_{DDQ} in which the leakage current is observed as a function of another parameter (temperature, voltage, test pattern etc.).
- Dynamic current-based tests or transient current testing (I_{DDT}).

Of course the best PPM figures are achieved if one would apply all tests. However each test has a cost aspect.

For example delay fault testing requires more test patterns and therefore more test time than SAF testing. While current-based tests use a smaller number of test patterns than static voltage testing but require additional hardware to measure the currents. It is therefore important to know what kind of test-mix is needed to obtain the required quality level at the lowest cost. To properly address this mix one needs to know the probability of occurrence of a particular defect type and how well this type of defect is detected with one of the four classes of test methods. This last part of the question is addressed in this paper. An estimation of the defect detection capabilities of the four classes of test methods is given for a 0.25 μm technology. One of the important effects one encounters in deep sub-micron technologies is process variation. This paper shows how this affects the test methods.

The remainder of this paper is organised as follows. Section 2 presents related research. In section 3 simulations are performed to investigate how the four classes of test methods perform for opens and shorts. Section 4 addresses the important issue of process variation and how this affects the defect detection capabilities. The paper is concluded in section 5 with the conclusions.

2 Related work

How well certain test methods perform has always intrigued the test community and a lot of excellent theoretical and experimental work has been published. One of the major experimental studies in the last years was the SEMATECH “Test Methods Evaluation” study S-121 [6]. In this study they compared SAF, I_{DDQ} and delay fault tests applied via scan chains together with a functional test applied via the I/O pins. Their main observations were that on one hand a large fraction of devices is detectable by almost all methods and thus apparently contain a major flaw while on the other hand a lot of the devices are only detectable by a single method and thus contain very specific faults. These findings are in agreement with other experimental studies [7][8].

Hawkins *et al.* [9] distinguished three general categories of defects: bridge, open circuit, and parametric defects. Although the number of breaks and bridges that can occur are roughly equal, practice shows that shorts are still the dominant defect for mature manufacturing processes [10]. This is due to presence of particles, which can cause shorts and the use of positive photoresists. Only a few experiments have been performed to obtain statistical data of the electrical characteristics of defects. The study of Bruls [11] showed that most of the bridging defects had small resistances well below 100 Ω but that a fraction of them does have resistances well above 10 k Ω .

Vierhaus *et al.* [12] investigated the impact of resistive shorts and opens on voltage testing (both dynamic

and static) and on static current testing in a combination of 1.5 and 2.5 μm technologies. Their results showed that I_{DDQ} testing is by far superior as test method for detecting shorts and that delay fault testing outperforms the other methods for detecting opens. The impact of a defect on the circuit depends on the characteristics of a defect. Therefore the detectability range was divided in large delays and fine delays for dynamic voltage-based testing and gross and fine leakage currents for static voltage testing. The detectability of fine delays and small leakage currents depended on the test equipment. They did not address the testability of parametric faults nor the impact it will have on the defect detection capabilities of a method.

3 Simulation results

The results of Vierhaus *et al.* are based on a ~ 2 μm technology. Furthermore dynamic current-based testing was not included in their simulations and it is interesting to investigate how this method performs compared to other methods. Therefore spice-like simulations with simple defect models are performed to provide an indication how well each class of test methods performs in detecting shorts, opens and parametric faults in a 0.25 μm technology.

A remark has to be made about dynamic current testing or transient current testing. Since it only emerged recently there exist quite diverse implementations of the method. The methods vary from integrating the current during the transition [13] and thereby losing the information of the shape of the transient current waveform, to sampling the complete waveform with a high-speed digitizer [14]. The defect detection capabilities of the method of course depend on the way it is implemented. Within Philips a transient current test method is investigated which uses a band-pass filter to transform the waveform [15]. This transformation allows us to obtain information about the shape of the waveform while still using only one sampling moment per transition. This method is capable of detecting resistive shorts between signal lines of 100 k Ω in leaky deep sub-micron technologies. Experiences with our implementation are used to grade dynamic current-based testing with respect to the other methods in the coming analyses.

3.1 Shorts

Vierhaus *et al.* investigated three types of shorts: an input-input bridge, an input-output bridge and a “stuck-on” defect. Input-input bridges in a NAND will not cause stuck-at faults for dominant n-networks, as is the case for conventional standard cells. The behaviour of an input-output short and a “stuck-on” fault appears to be comparable. Therefore the “stuck-on” defect denoted with R_{BRIDGE} in Figure 1 is investigated. The resistance of this

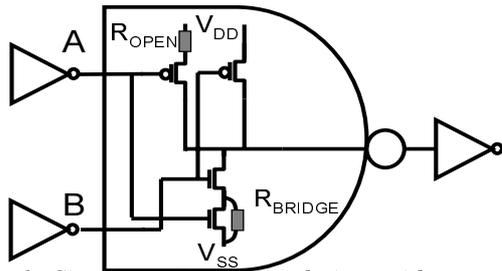


Fig. 1: Circuit used in the simulations with two types of defects R_{BRIDGE} and R_{OPEN} .

short is varied between 100Ω and infinity. The defect will affect the output signal of the NAND for a transition of input A from high to low as is shown in Figure 2a. All kinds of intermediate output voltages will occur. However, after one additional gate the signal is again defined for almost all resistances as either high or low (see Figure 2b). The resistance interval for which this transition occurs is quite narrow. Stuck-at faults occur for resistances up to $1 \text{ k}\Omega$ while for resistances above $3 \text{ k}\Omega$ the impact on the output voltage of the inverter is negligible. However it should be stressed that although the defect does not affect the logic, the device still contains a flaw. A defect can evolve over time due to electromigration or stressing. A small change in the defect characteristics can change the resistance and suddenly a “good” device starts to malfunction.

The determined threshold resistance for stuck-at faults is $1 \text{ k}\Omega$. This is smaller than the values found in the study of Vierhaus *et al.* They determined a threshold re-

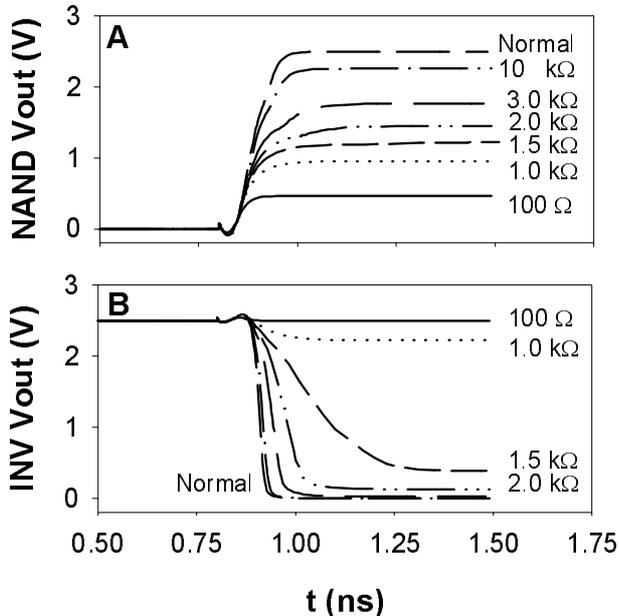


Fig. 2: Response of a) the NAND gate and b) the last inverter stage for a falling transition on A for R_{BRIDGE} values between 100Ω and infinity.

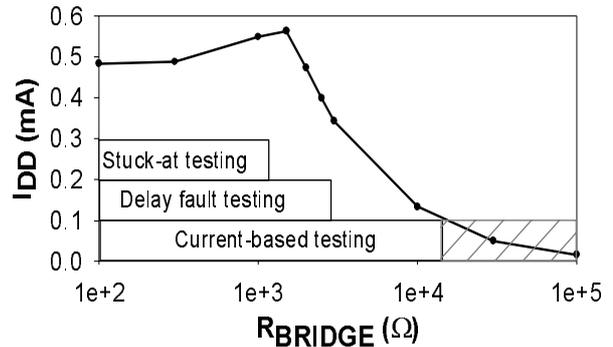


Fig. 3: I_{DDQ} current as a function of resistance and the detection range of SAF testing, delay fault testing, I_{DDQ} testing and advanced current-based test methods (hatched area).

sistance of $6 \text{ k}\Omega$ in a $\sim 2 \mu\text{m}$ technology and of $4 \text{ k}\Omega$ in a $\sim 1.2 \mu\text{m}$ technology. The sudden transition from faulty behaviour to good behaviour also means that dynamic voltage-based tests are only slightly better in detecting shorts than static voltage-based tests. The detection limit for delay fault testing is around $3 \text{ k}\Omega$.

Instead of the impact on the voltage one can also observe the current of the power supply. For a single gate under static conditions this current is very small. However due to the defect an additional current will flow. The magnitude of this current depends on the resistance of the defect (see Figure 3). Leakage currents of $1 \mu\text{A}$ used to be detectable with I_{DDQ} testing. However, the increase in leakage current for deep sub-micron technologies has made the method less effective. For $0.25 \mu\text{m}$ technologies additional currents of $100 \mu\text{A}$ are still very well detectable with an I_{DDQ} test with a single limit. Moreover, new methods like ΔI_{DDQ} testing and I_{DDT} testing can detect leakage defects of $10 \mu\text{A}$ in leaky technologies and therefore $\sim 100 \text{ k}\Omega$ defects are still detectable with current-based tests.

The capabilities of Philips’ transient current test method to detect shorts in $0.25 \mu\text{m}$ technologies are slightly worse than those of advanced static current-based test methods. Our I_{DDT} test method is insensitive for steady state leakages and is therefore not capable to detect shorts between power supply lines. Furthermore, if we compare the capabilities to detect shorts between signal lines than ΔI_{DDQ} is capable of detecting smaller leakage defects than transient current testing. However static current-based test method will be hampered by the increase in sub threshold leakage and it is quite possible that for $0.12 \mu\text{m}$ technologies the dynamic current-based test methods are better in detecting shorts than static methods.

In Figure 3 also the detection range of SA testing and delay-fault testing is marked. The capabilities of delay fault testing are slightly better than those of static

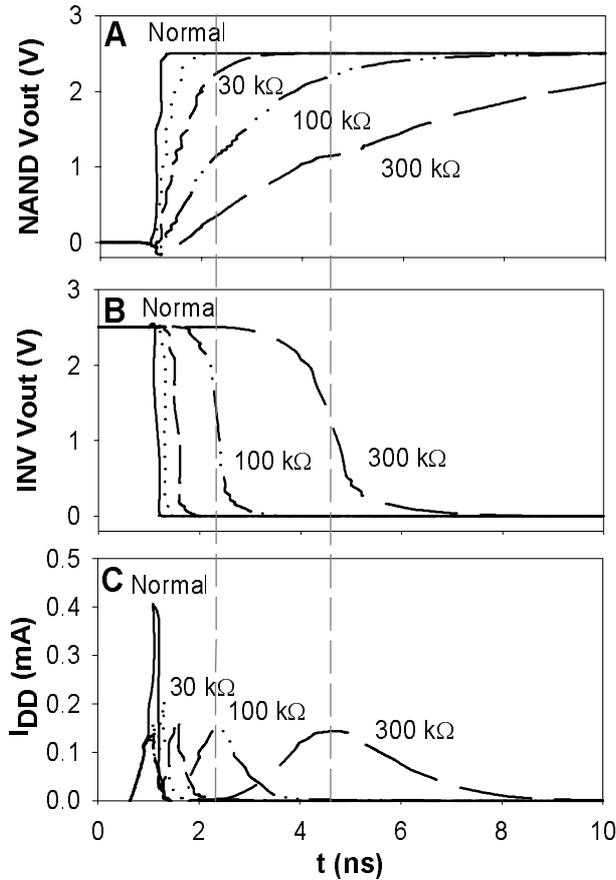


Fig. 4: Response of a) the NAND output and b) the last inverter stage c) the I_{DD} current for several values of R_{OPEN} (dotted line is for 10 k Ω).

voltage-based testing as is shown in Figure 2b. I_{DDQ} testing with a single limit is still much better in detecting shorts than voltage-based test methods. Advanced current-based test methods can extend the detection range even further.

3.2 Opens

To investigate the capabilities of the four test methods to detect an open, the R_{open} defect in Figure 1 is analysed. The defect model consists of a resistor between the power supply and the source of a p-transistor. Quite often other models are used. Breaks in signal lines are usually modelled with capacitors. This model was for example used in the studies of Rodriguez-Montanes *et al.* [16] and Renovell and Bertrand [17]. Although the details will be different, the behaviour is identical. In general the defect will slow down transitions. However, under static conditions the correct output voltage will often be obtained due to the (slowly) charging of nodes. This behaviour makes dynamic test methods better suited to detect open defects.

Figure 4a shows the response of the output of the NAND for several resistances. As for the bridging defect

the impact of the defect is reduced after the inverter stage (see Figure 4b). However, considerable delays are now observable. For example a R_{OPEN} of 300 k Ω results in an additional delay of 5 ns. This defect cannot be detected with static voltage testing but is detectable with delay fault testing.

Opens are often also detectable with current-based test methods owing to intermediate voltage levels at the output of the gate. While the output gate is floating between $V_{SS} + V_{TN}$ and $V_{DD} - V_{TP}$ both the n-transistors and the p-transistors can conduct and an increased I_{DD} current is observed. These conditions can also occur for shorts. However, the big difference is that for shorts the conditions are usually static while for opens the conditions are dynamic. Therefore it is for open defects no longer possible to observe the impact of the defect at an arbitrary moment and the detection by static methods is uncertain. Figure 5c shows the dynamic character of the I_{DD} current for several R_{OPEN} values. The maximum of the I_{DD} current is, just like the transition, delayed and will occur when the output passes $V_{DD}/2$. Furthermore, the increased leakage can only be observed in a specific time window. For example for an R_{OPEN} of 300 k Ω the I_{DD} current is again below 5 μ A within 10 ns. A leakage current measurement after 10 ns will not reveal the defect. This immediately shows why dynamic current-based testing will perform better than static current-based testing in detecting opens.

Besides the time shift the defect has a second impact on the I_{DD} current; the current will flow during a prolonged period making the total power consumption slightly larger. Dynamic current-based methods which can observe these time shifts and/or power consumption changes, can detect opens just like dynamic voltage-based methods. However, delay fault testing targets only one gate while current-based tests observe all gates together. This is an advantage for I_{DDQ} testing since all other gates are quiet and it is easy to detect the impact of the defect. However, in a dynamic current test, a large fraction of the gates are switching. This makes it harder to distinguish the effect of the defect. The impact of the defect is small compared to the total power consumption during an active edge. Methods, which retain information about the waveform, are most likely better in the detection of opens due to the detectability of the postponed transition.

In summary opens are hard to detect with static methods. Dynamic test methods are capable of detecting opens. The occurrence of a delay fault implies a change in the I_{DD} signature and therefore the defect is theoretical detectable by a dynamic current test. However, the effect is small compared to the total activity of a device, which makes the method in general less suited to detect small delays defects. Theoretically dynamic voltage-based test-

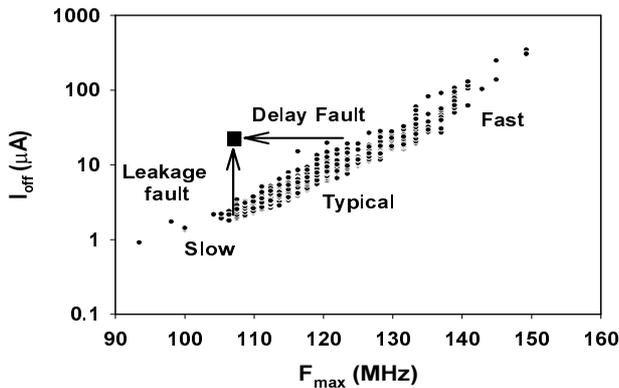


Fig. 5: Relation between process variation, the maximum speed (F_{max}) and the leakage current (I_{off}) together with a typical defect (black square).

ing will perform better than dynamic current-based testing for opens.

3.3 Parametric faults

The previous two categories of defects are local defects, which only affect a few transistors. Parametric faults, however, are global effects, which affect large areas of a wafer and are caused by unintentional shifts in the processing. Process variation is usually well detectable by the use of process control modules. However, for deep sub-micron technologies the fear arises that intra-die parametric faults become important. These “faults” will be missed by process control modules since the impact is very local.

Intra-die effects, which affect the speed are detectable by test methods such as path-delay testing. Like gate-delay testing the test method determines the additional delay due to defects. The main difference is that gate-delay testing targets a defect, which has an impact on a single gate while path-delay testing targets all gates along a path. Therefore path-delay testing is capable of detecting area “defects” or parametric faults, which have a small impact on a single gate but are detectable if several gates on a single path are affected and therefore degrade the performance of a device.

The first impression would be that current-based tests are not capable of detecting parametric faults or process variation. However in Section 4 it is shown that V_T variation has a big impact on the leakage current. Therefore current-based tests can be used as indicators of process shifts which affect V_T 's.

4 Effects of process variations

Based on the results of the previous section it seems that not much has changed in the last decade; dynamic methods are still good in detecting opens while current-based tests are still good in detecting shorts. However,

one aspect of the test method has changed dramatically. The limitations to detect a defect are no longer determined by the measurement equipment itself but by how well the method can cope with process variation. Short-channel effects and process shifts have a big impact on the leakage current. First it was assumed that the increase in magnitude of the leakage current would be the main problem for current-based testing. However, it turned out that the main problem is the variance in leakage current owing to process variation [18]. Figure 5 shows an example of why I_{DDQ} testing with a single pass/fail limit will lose its effectiveness in deep sub-micron technologies. The data plotted in Figure 5 is based on data acquired for a device with 180k gates, made in a 0.25 μm technology. The F_{max} figure is determined by applying delay fault test patterns and gradually increase the capture speed in steps of 0.1 ns. The speed just below the speed for which incorrect data is captured, is considered as F_{max} . This is not the real operational speed but it is very useful as a figure of merit.

Data is available for three kinds of processes, which are denoted as “slow”, “typical” and “fast” processing in Figure 5. Data is not acquired from a real “Maverick” lot but it shows the kind of process variations one could encounter. Only a limited number of slow devices were available and therefore the slow region is not as densely populated as the typical and fast regions.

Process variation effects the threshold voltage and thereby the speed and the leakage current. The effect of V_T variation is more or less linear on the speed but exponential on the leakage current. A slow device will have a leakage current of $\sim 1 \mu\text{A}$ while a twice as fast device has a leakage current of $\sim 1 \text{mA}$, three orders of magnitude more! This shows why single limit I_{DDQ} testing is not effective any more for deep sub-micron technologies. Typical additional leakage currents due to defects are in the order of $10 \mu\text{A}$ to several mA. The black square in Figure 5 represents a defective device. To detect this device one would need a low I_{DDQ} limit of $20 \mu\text{A}$. However this limit also results in the rejection of many good devices and therefore has a profound impact on yield. A high I_{DDQ} limit of $100 \mu\text{A}$ has a much smaller impact on yield but will also miss a lot of devices with defects and therefore results in a deterioration of the quality level.

Figure 5 shows that test methods for deep sub-micron have to be robust to process variations. Relative methods like ΔI_{DDQ} [19] and I_{DDT} [20] can cope with this variance. Although the problem of process variation is more severe for current based testing due to its exponential dependency, the problem also exists for delay-fault testing. A speed difference of a factor of one-and-a-half could exist between fast and slow devices. To detect defects, which add a small delay one needs a delay fault

method which can cope with the effects of process variation. The black square in Figure 5 can also be a device with a delay fault of 2 ns. If one uses a single limit for delay fault testing this defect is missed. Although the defective device will perform according to the minimum specification it still contains a defect, which affects its performance and is a reliability risk.

5 Conclusions

A comparison is made between the defect detection capabilities of the four classes of test methods for three categories of defects. The simulations are made with simple models of defects that by no means resemble the sometimes complex behaviour of real defects. However they provide valuable insight in the capabilities of a test method. For the detection of shorts, current-based tests are still superior to voltage-based tests. However, the detection limits for shorts have decreased for all test methods and the increase in sub-threshold leakage will hamper current-based test methods. Since shorts are still the dominant defect it is therefore important to continue the development of new current-based tests to retain the present quality level. For opens and parametric faults dynamic voltage-based methods have the best defect detection potential. However, they require two different types of implementation. For opens one wants to target short paths (ideally one gate) while for parametric faults one wants to target a long path.

An important issue for all test methods is how well they can cope with process variation. The impact of process variation can mask defects and the detection of a defect with a small impact is no longer determined by the measurement equipment but by the capability of the test method to cope with this variations. The mentioned advanced current-based methods have this capability.

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