LEAP: An accurate defect-free I_{DDQ} estimator

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Abstract - *The quiescent current (I_{DDQ}) consumed by a CMOS IC is a good indicator of the presence of a large class of defects. However, the effectiveness of I_{DDQ} testing requires appropriate discriminability of defective and defect-free currents, and hence it becomes necessary to estimate the currents involved in order to design the I_{DDQ} test. In this work, we present a method to estimate accurately the non-defective I_{DDQ} consumption based on a hierarchical approach at electrical (cell) and logic (circuit) levels. This accurate estimator is used in conjunction with an ATPG (Automatic Test Pattern Generation) to obtain vectors having low/high defect-free I_{DDQ} currents.*

1 Introduction

I_{DDQ} testing has become a widely accepted defect detection technique in CMOS IC testing [1]. It is based on the fact that ideally a non-defective CMOS circuit has a quiescent current much lower than the defective one. However, for present and future high speed CMOS technologies, the discrimination of the defective and the non-defective I_{DDQ} currents is becoming more critical due to the manufacturing improvements which have led to a reduction in the minimum feature size as well as an increase in chip sizes [2],[3],[4].

This fact questions the validity of performing I_{DDQ} testing against a single threshold value [5]. Some methodologies have been proposed to avoid this problem. In most of these methodologies, evaluation of defect-free I_{DDQ} is required [6], [7].

We have developed an *accurate hierarchical estimator* tool, called LEAP, to estimate defect-free quiescent current for a given input vector. Since defect-free quiescent current of 'OFF-state' transistors depends on the internal voltages of each cell, the computation is carried out both at electrical and logic levels. This accurate estimator is used in conjunction with an ATPG (Automatic Test Pattern Generation) tool to obtain the vectors having low/high defect-free I_{DDQ} currents which may be also useful to design the I_{DDQ} test [8]. In this way, if design requirements on defect-free quiescent power consumption are not met, the design may be changed at early stages of the project by using a different library or reevaluating the defect-free quiescent power goal.

The present approach is more general than current alternatives. Gu and Elmasry [9] introduced a simple analytical model for estimating leakage current at transistor level. Their model is based on using process specification, leakage current equations from BSIM transistor model and Kirchoff's Laws. The leakage current for basic CMOS cells, assuming NMOS and PMOS to be equal, was obtained.

Maxwell and Rearick [10], [11] presented an alternative approach to use a switch level simulator to determine the configurations of 'ON-state' and 'OFF-state' transistors, and estimate defect-free quiescent based on this information. This method avoids any characterization requirement, but the mapping of transistor information to defect-free quiescent currents needs adjustable parameters in a post-simulation step.

Roy et al. [12], [13] presented an approach using process specification, leakage current equations and Kirchoff's laws to evaluate the leakage current of a cell. Using the BSIM model, they derived an accurate model to predict quiescent voltages and leakage current in a stack of transistors. This implementation assumes a conventional CMOS logic style in which steady-state gate voltages are V_{DD} or 0 V.

The rest of the paper is structured as follows: Section II presents the hierarchical I_{DDQ} estimator. Section III presents the method to find vectors producing low/high defect-free I_{DDQ} using a standard ATPG. Section IV validates the results using Monte-Carlo Simulation for ISCAS'85 benchmarks. Finally, the conclusions of the work are presented.

2 LEAP. A Hierarchical I_{DDQ} Estimator

The estimation of non-defective I_{DDQ} distribution requires information on technology parameters, circuit topology, temperature, power supply, circuit input and memory state.

LEAP is an automatic estimator of I_{DDQ} for a given input vector. This method is based on a hierarchical estimation at two levels: at a cell level (electrical) and at a circuit level (logic).

2.1 Cell Level

At cell level, the current consumption depending on the input vector for each cell in the library is obtained for the corresponding operating conditions. The characterization is performed at electrical level using HSPICE. Of course, this approach depends on the matching between the HSPICE models and the fabricated MOSFETs. Usually, the foundries themselves provide device models of their technology such as Berkeley's Model (BSIM3v3).

The dependence of defect-free quiescent current on operating conditions, such as voltages and temperature and design parameters, such as channel length and width, is embedded in the HSPICE device model. Usually, analytical and experimental methods are used with fixed values of channel length and other parameters. However, in some cells, such as latches, different transistors may have different topologies. In addition, HSPICE simulation allows the defect-free quiescent current inside a cell to be evaluated for any style of CMOS logic (i.e. cells with pass transistors where the gate voltages may deviate from the conventional V_{DD} and 0 levels). Usually, state of the art I_{DDQ} estimators are able to deal only with full-complementary CMOS cells.

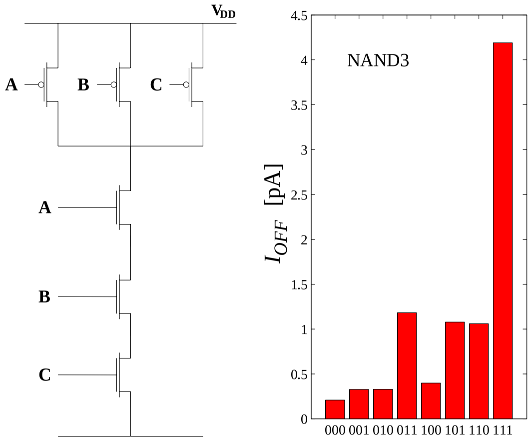

Figure 1: Defect-free I_{DDQ} in a 0.5 μm three-input NAND cell

In order to illustrate the characterization method, let us consider a three-input NAND cell. In Figure 1, the defect-free quiescent current depending on the input for a 0.5 μm technology three-input NAND cell at room temperature and $V_{DD} = 3.3$ V is presented. The first bit corresponds to the input closest to the output and the third bit corresponds to the input closest to the ground rail.

Let us analyze the behavior of the NAND cell. The inputs 000-110 produce an output equal to '1'. Therefore, the defect-free quiescent current is controlled by the NMOS network. For these inputs, I_{OFF} currents are seen to group into two major classes: The high I_{OFF} group consists of states 011, 101, and 110. These states have a single 'OFF-state' NMOS with drain and/or source connected through an 'ON-state' NMOS to a power rail. The small differences between these states are due to the different voltages between drain and source terminals. The other states, 000, 001, 010, and 100, have more than one NMOS in 'OFF-state'. Differences in currents within this group depend on the number of 'OFF-state' transistors (2 or 3) and the voltage at the edges of these pulldown stacks. The input 111 produces an output equal to '0' and the defect-free quiescent current is simply the sum of the defect-free quiescent current of the PMOS transistors.

HSPICE simulations can be automated easily to generate I_{DDQ} consumption tables for the cells in one library. The HSPICE pre-characterization is performed only once for each library and is performed in execution times in the order of the number of cells in the library. This information is then used to obtain the I_{DDQ} current of a whole circuit.

2.2 Circuit Level

At circuit level, the defect-free quiescent current of the whole circuit is computed as the sum of the defect-free quiescent current of each cell in the circuit. First, using a logic simulator the values of internal nodes are obtained. Then, for each cell in the circuit, the defect-free quiescent consumption for the corresponding local input values is obtained from the set of pre-characterized I_{DDQ} consumption tables. Finally, the sum of all these values gives the total defect-free quiescent current.

The LEAP tool has been used to characterize the defect-free quiescent current of a set of combinational circuits (ISCAS'85) for nominal values of process parameters. These circuits have been implemented using a 0.5 μm technology. The histogram obtained for circuit 1908 is indicated in Figure 2.

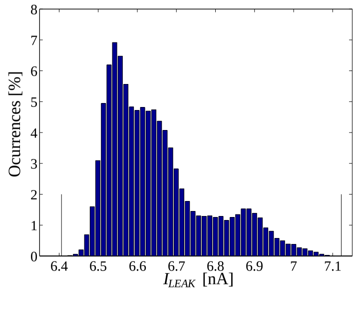

Figure 2: Sample histogram of I_{DDQ} of ISCAS'85 c1908 circuit

Note that in the case of circuit 1908 the distribution does not approach a Gaussian distribution. The histogram obtained for circuit c5315 is indicated in Figure 3.

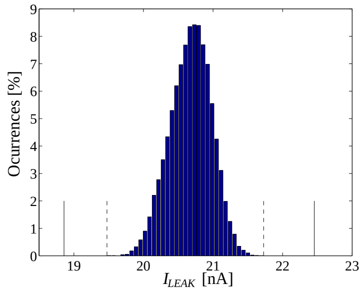

Figure 3: Sample histogram of I_{DDQ} of ISCAS'85 c5315 circuit

Hierarchical estimation is able to obtain precise estimations of defect-free quiescent consumption with execution times of the order of the logic simulator time. HSPICE simulation of the whole circuit (which produce results equal to the ones obtained by this method) is impractical in large size designs.

3 Maximum and Minimum I_{DDQ} of a CUT

In I_{DDQ} test strategies using variable threshold values, it is useful to know the maximum and minimum values of defect-free I_{DDQ}, depending on the input vector v. This may be a hard task, since finding the exact maximum or minimum I_{DDQ} and the vectors producing them is an NP-complete problem.

Only in small circuits and some special cases, it is possible to find exactly the maximum and minimum I_{DDQ}. For large circuits, an alternative approach is to develop methodologies (or heuristics) in order to find input vectors producing near maximum and minimum leakage current.

In this section, a Hierarchical methodology to find maximum and minimum defect-free quiescent current using LEAP and a commercial ATPG tool is presented. This methodology is based on precomputing the defect-free quiescent current of CUT modules defined by adequate partitions of the circuit. Subsequently, we try to set the CUT in high (low) defect-free quiescent current state with a global input vector using a commercial ATPG tool. To evaluate the goodness of the results obtained, i.e., how close are the estimated maximum and minimum leakage currents obtained using these methodologies to the real values, upper and lower bounds of the actual maximum and minimum values of the leakage current are obtained as shown in Figure 4. The measure of quality of the estimation is related to the difference between these bounds.

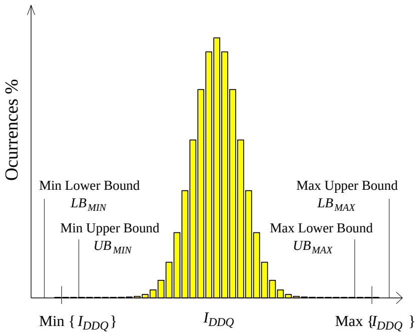

Figure 4: I_{DDQ} Histogram as the input vector changes

3.1 ATPG-based methodology

In this section we present the ATPG-based proposed approach to find a reachable lower bound of maximum and an upper bound of minimum dfect-free I_{DDQ} current. Let us to consider the case of finding an upper bound of the minimum I_{DDQ}. Equivalent reasonig leads us to find a lower bound of the maximum I_{DDQ}.

The structure/functionality of a CMOS circuit is described hierarchically at different levels. At RTL level, the circuit is specified using medium size blocks. The I_{DDQ} current of these blocks can be efficiently precharacterized. Other blocks have to be partitioned until each partition can be efficiently precharacterized.

For each partition, a multiple-output logic function which we call *estimator* is generated. This function is produced by auxiliary cells associated to each partition and producing an output estimating the I_{DDQ} of the corresponding partition. The I_{DDQ} current is discretized in two intervals and the output codifies the interval. If the input vector applied to the partition produces an I_{DDQ} which achieves a certain margin below the absolute minimum I_{DDQ} of the partition, the output of the corresponding auxiliary cell is '1'. Otherwise the output is '0'. Then, I_{DDQ} consumption is codified using two values (high, low). For instance, the estimator of minimum defect-free I_{DDQ} current of the three-inputs NAND gate in Figure 1 is a NOR gate, as shown in Figure 5.

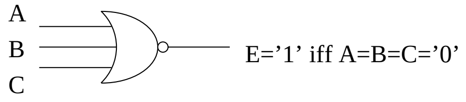

Figure 5: Minimum I_{DDQ} estimator of a three-input NAND gate

The outputs of all the estimators are used as objectives by the ATPG to obtain input vectors with low I_{DDQ}. An adequately chosen subset of objectives (i.e. the outputs of the estimators) is applied to an AND gate. This AND gate serves to check their compatibility, i.e. if it is possible to set these

outputs to the desired value at the same time.
Any vector detecting a stuck-at-0 at the output of the AND gate will set the outputs of the estimators to '1', and the corresponding associated partition will be in a low defect-free quiescent state. Therefore, the input vector of the whole circuit found will produce a low I_{DDQ} current. If no vector is found or the quality of the result is not good enough, the estimators should be modified in order to be less restrictive by allowing more input vectors to produce a '1' at the output of the estimator.

3.2 Search algorithm

The search algorithm tries to achieve some objectives simultaneously. These objectives correspond to the allowed states of each partition producing a '1' at the output of the corresponding I_{DDQ} estimator. The list of objectives to cover simultaneously is used as the input to a greedy algorithm. The greedy algorithm has the following objective: to maximize the number of partitions which are in a low defect-free quiescent state. If the circuit is partitioned in such a way that all the partitions are independent, the algorithm produces the minimum I_{DDQ} value. Unfortunately, for most circuits, the independence assumption does not hold, but if the partitions are sufficiently large, with high correlations inside a block and low correlations between blocks, the heuristic has been found very efficient.
First, the blocks are first sorted according to their size. In this way, a larger fraction of the circuit is close to the desired consumption. This list of objectives to satisfy simultaneously is used as the input to the following greedy algorithm:

1. *Take two objectives from the top of the list and use the corresponding outputs of the estimator as inputs to the AND gate.*
2. *Run the ATPG to detect a stuck-at-0 at the output of the AND gate.*
3. *Evaluate the number of objectives covered.*
4. *If the stuck-at-0 has been detected, include a new objective (i.e. a new output of function E) from list S and return to step 2.*
5. *Else, exclude the last objective, modify it to be less restrictive by allowing more states to produce a '1' at the output of the estimator and return to step 2.*
6. *Stop the algorithm when all the objectives in the list have already been attempted.*

Notice that this method always gives a reachable lower bound of maximum or upper bound of minimum, and the vector producing the corresponding value.

3.3 Upper Bound of Maximum I_{DDQ} (Lower Bound of Minimum)

To obtain a lower bound of minimum and an upper bound of maximum defect-free quiescent current consumption by the circuit, a strategy based on dynamic programming is used. The structure and functionality of the circuit is used to generate an equivalent constrained graph. The problem of finding the vector producing maximum or minimum defect-free quiescent power consumption is reduced to the problem of finding the optimal-cost path joining two nodes in the graph. The optimal-cost path problem can easily be explained: given a network in which each arc has an associated cost, find an optimal-cost path to a specified node (sink) from another node (source). The associated cost of the arcs is related to the IDDQ of each cell with the corresponding inputs.
If the number of internal nodes is low, the number of states (vertices) is relatively small and this method also allows the vectors producing the maximum or minimum defect-free quiescent value to be found exactly. However, if the circuit has a large number of internal nodes, the number of states (vertices) in the graph may grow exponentially, and therefore, the method will be unable to find the exact solution in a reasonable amount of time.
A possible solution is to break the circuit into partitions leaving the nodes on the frontier of the partition unconstrained and applying dynamic programming (or simulating if the partition is small enough) to each partition. This leads to a result which is an upper bound of maximum (lower bound of the minimum) defect-free quiescent .

4 Validation and Experimental Results

The hierarchical methodology of computation of the lower bound (upper bound) of the maximum (minimum) has been incorporated into the software tool LEAP (LEAkage Power Estimator). In this section, the lower and upper bounds of the maximum and minimum defect-free quiescent currents of some benchmark circuits are presented. The results obtained are compared with the results obtained with pseudorandom simulations of 100,000 vectors. The cost of each method is given in terms of CPU time[seconds] on a UltraSparc1 workstation. For pseudorandom simulations this cost is evaluated as the time needed to simulate all the vectors applied to the circuit plus the time needed to compute the values of defect-free quiescent current. For the LEAP tool, this cost is evaluated as the time needed to simulate and compute the defect-free quiescent current of all the vectors for each different block plus the execution time of the heuristic, which includes the ATPG running time.

Results for estimation of maximum and minimum defect-free quiescent values using LEAP and using Monte Carlo simulations are compared in the following tables. In tables 1 and 2, the results obtained when searching for maximum and minimum I_{DDQ} using LEAP and Monte Carlo simulation are presented.

The proposed method has a significantly higher efficiency than Monte Carlo simulations. The reduction in the computation times is around 20-25 times for all the circuits, both for maximum and minimum cases, except for one circuit. For the c6288 circuit, the reduction in the computation time is 56 times for the minimum case and 60 times for the maximum case. Notice that in all cases, the results obtained using LEAP are better than those using Monte Carlo simulations.

Table 1: Results of lower bound of maximum I_{DDQ} computation

	LB_{MAX} [pA]		CPU time [s]		Speed Up
Circuit	LEAP	Random	LEAP	Random	
c432	1924.6	1868.2	23.2	470.8	20.3
c499	3093.9	3074.1	30.7	636.7	20.7
c880	3847.3	3752.6	44.7	1061.4	23.7
c1355	3093.9	3074.1	31.0	636.7	20.5
c1908	7122.0	7093.1	94.8	2402.0	25.3
c2670	11814	11644	139.8	3299.2	23.6
c3540	15449	15345	184.8	5001.7	27.0
c5315	22456	21727	290.7	6818.0	23.4
c6288	22561	22257	337.4	20307	60.2
c7552	31701	30795	435.8	10529	24.2

Table 2: Results of upper bound of minimum I_{DDQ} computation

	UB_{MIN} [pA]		CPU time [s]		Speed Up
Circuit	LEAP	Random	LEAP	Random	
c432	1399.4	1424.1	20.6	470.8	22.8
c499	2663.4	2714.3	32.4	636.7	19.7
c880	2874.1	2977.3	49.3	1061.4	21.5
c1355	2663.4	2714.3	32.7	636.7	19.5
c1908	6405.9	6430.3	100.6	2402.0	23.9
c2670	10866	10982	159.3	3299.2	20.7
c3540	13668	14030	211.2	5001.7	23.7
c5315	18858	19476	322.4	6818.0	21.1
c6288	20444	20593	362.6	20307	56.0
c7552	27040	28247	495.4	10402	21.0

In general, for very large circuits, the structural dependence between cells and therefore, between the defect-free quiescent current of these cells, is known to decrease with the distance (in terms of levels) between the gates. Then, if the circuits are large enough, defect-free quiescent current distributions would be expected to be (truncated) Gaussian or nearly Gaussian. Actually, this is observed for all the benchmark circuits experimented, except for c1908 and c6288.

The values further away from the mean ± 3σ are very unlikely but are (usually) reachable for some input vectors. In other words, if the circuit is large enough, some parts of the circuit will act as if they were independent from other parts in the circuit. Therefore, they may be set *independently* in a certain logic state producing some defect-free quiescent consumption. This task may be achieved using the ATPG efficiently because the search is directed to certain logic states, which in turn may be very unlikely. On the other hand, Monte Carlo simulation is inefficient to find these states with very low probability.

The two circuits where there is no (or small) improvement are circuits with highly correlated structures. Circuit c6288 is an array 16×16 multiplier with a high internal reconvergence. Circuit c1908 is a 16-bit single-error-correcting and double-error-detecting (SEC/DED) circuit with some byte-error detection capability. It generates a 6-bit syndrome from the 16-bit data input, which is decoded to find the bit in error. A large part of the circuit is devoted to syndrome decodification and error correction and therefore depends only on a few bits. As a consequence, a large number of input vectors sets a large part of the circuit in high/low consumption states.

In tables 3 and 4, the upper bound of maximum defect-free quiescent (UB_{MAX}) and the lower bound of maximum defect-free quiescent (LB_{MAX}), and the upper bound of minimum defect-free quiescent (UB_{MIN}) and the lower bound of minimum defect-free quiescent (LB_{MIN}) are presented.

The maximum defect-free quiescent current is estimated using the following expression

$$\hat{I}_{DDQ}^{MAX} = \frac{UB_{MAX} + LB_{MAX}}{2} \tag{1}$$

The maximum error in the estimation is given by the following expression

$$Maximum\,Error\ (\%) = \frac{UB_{MAX} - \hat{I}_{DDQ}^{MAX}}{\hat{I}_{DDQ}^{MAX}} \cdot 100 \tag{2}$$

The results show that this error is always found to be lower than 8%, and for the two largest circuits is lower than 1.3%. These errors are low because the blocks in which the circuit has been partitioned are allowed to be only in a narrow interval of consumption around maximum (or minimum) values by the estimator. Using the ATPG, we make sure that a large fraction of the blocks in the circuit is in these high consumption states. Furthermore, since highly correlated nodes are kept inside the same partition, the difference between the defect-free quiescent current of the block with and without unconstrained inputs should be small.

Table 3: Error in max. I_{DDQ} estimation using LEAP. Lower and Upper Bounds are given in [pA]

Circuit	LB_{MAX}	UB_{MAX}	$\hat{I}^{MAX}_{LEAK}$	Max. Error
c432	1924.6	1991.5	1958.0	1.7 %
c499	3093.9	3264.7	3179.3	2.7 %
c880	3847.3	4319.1	4083.2	5.8 %
c1355	3093.9	3264.7	3179.3	2.7 %
c1908	7122.0	7587.5	7354.8	3.2 %
c2670	11814	12256	12035	1.8 %
c3540	15449	17075	16262	5.0 %
c5315	22456	23442	22949	2.2 %
c6288	22561	22561	22561	0.0 %
c7552	31701	32537	32119	1.3 %

Table 4: Error in min I_{DDQ} estimation using LEAP. Lower and Upper Bounds are given in [pA]

Circuit	LB_{MIN}	UB_{MIN}	$\hat{I}^{MIN}_{LEAK}$	Max. Error
c432	1242.1	1399.4	1320.8	5.9 %
c499	2663.4	2663.4	2663.4	0.0 %
c880	2565.7	2874.1	2719.9	5.7 %
c1355	2663.4	2663.4	2663.4	0.0 %
c1908	5986.4	6425.8	6206.1	3.5 %
c2670	9568.5	10866	10217	6.4 %
c3540	11693	13668	12680	7.8 %
c5315	17236	18858	18047	4.4 %
c6288	20444	20444	20444	0.0 %
c7552	26986	27040	27013	0.1 %

5 Conclusions

In this work, we present a methodology in order to estimate the defect-free quiescent current of large CMOS circuits. The defect-free quiescent current of a CMOS circuit depends on operating parameters such as temperature and power supply voltage, design parameters such as topology of the circuit, cells structure and device sizes and the input vector applied to the circuit.

We have developed an *hierarchical* tool, called LEAP, to estimate defect-free quiescent current for a given input vector. The LEAP tool is based on a hierarchical estimation at cell level (electrical) using SPICE and at circuit level (logic) using a logic simulator. This implies a high accuracy with reduced execution times.

Using this accurate estimator, an ATPG-based methodology to evaluate the maximum and minimum defect-free quiescent current values is proposed. In addition, vectors producing high and low defect-free quiescent consumption are obtained. The results compare favorably with the state of the art in defect-free quiescent estimation.

Acknowledgment

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