Defect Detection from Visual abnormalities in Manufacturing Process Using I_{DDQ}

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Abstract

Abnormal I_{DDQ} *(Quiescent* V_{DD} *supply current) indicates the existence of physical damage in a circuit. Using this phenomenon, a CAD-based fault diagnosis technology has been developed to enhance the manufacturing yield of logic LSI. This method to detect the fatal defect fragments in several abnormalities identified with wafer inspection apparatus includes a way to separate various leakage faults, and to define the diagnosis area encircling the abnormal portions. The proposed technique progressively narrows the faulty area by using logic simulation to extract the logic states of the diagnosis area, and by locating test vectors related to abnormal* I_{DDQ}*. The fundamental diagnosis way employs the comparative operation of each circuit element to determine whether the same logic state with abnormal* I_{DDQ} *exists in normal logic state or not.*

1. Introduction

Although most of the visual abnormalities identified with wafer inspection apparatus (WIA) do not always become killer defects in LSI circuits because of efficient fabrication processes, some of these, however, do develop into fatal defects. In the past, a memory LSI consisting of a bit map occupied over 90% of the chip area made it possible to detect killer defects easily. This is because an arbitrary memory transistor was able to be simply assigned and its electrical characteristics were directly measured by indicating the address. A logic LSI consisting of various blocks made a fault detection difficult, because of low detection sensitivity and long measurement time based on traditional CAD-based diagnosis technology. This technology was typically conducted by using unexpected output data, being representatively a back tracing functional method and a fault dictionary method. Over 95% of total failures involve abnormal I_{DDQ}, and hence the fault diagnosis of logic LSI cannot be conducted without abnormal I_{DDQ} information [1]-[5]. The purpose of this paper is to present a diagnosis technique, which locates killer defects in the irregular portions detected by wafer inspection tools. Killer defect information obtained in this way can be fed back to logic LSI manufacturing processes, helping to improve manufacturing yield. The paper is organized as follows: Section 2 describes a simplified diagnosis flow and Section 3 presents a logic extraction of every block and line, composing LSI. Section 4 introduces an extraction of the test vector number (TVN) with various abnormal I_{DDQ} and next Section denotes the definition way of the diagnosis area adjusting the visual irregulars to the LSI layout portions. Section 6 details diagnosis technique with comparative operation technique. Section 7 presents the experimental results on actual faulty LSI chips with visual abnormalities, detected by WIA. This is followed by the conclusions.

2. Diagnosis flow

Figure 1 denotes a simplified fault diagnosis procedure. The diagnosis flow starting from the test vector extracts the expected input logic of each block and the logic state of every connection line between blocks, and the TVNs with abnormal I_{DDQ} through the LSI tester. On the other, the coordinates of each visual abnormality identified by the WIA are investigated. By using the above data, diagnosis areas encircle the coordinates of the visual abnormalities are defined, following which blocks and lines, *being downward designated as elements*, in this area are detected by LSI layout data. After that, each element is diagnosed in accordance with the following procedure, and the visual abnormal portions in diagnosis areas with the fault elements are judged to be fatal defects.

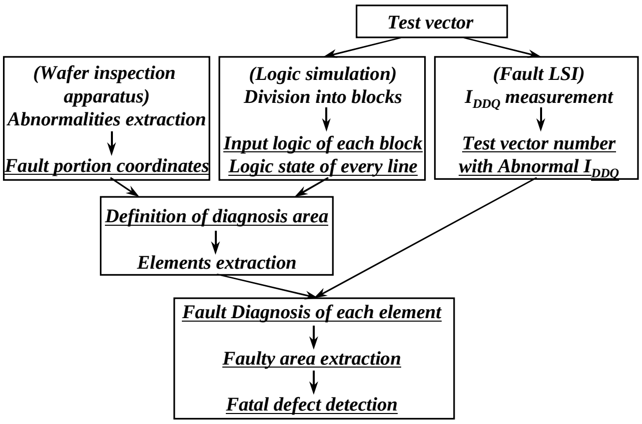


Fig. 1. A simplified fault diagnosis flow

3. Logic extraction of each element

The procedure shown in the center flow in Figure 1 is described for extracting the input logic of each block, and the logic state of every line. After the LSI circuit constructed using hierarchical design method is divided into functional blocks by net list and block library with a fundamental circuit behavior, the expected input logic of each block is extracted by logic simulation, a test vector and a net list. The expected logic state of each line is extracted next by using the net list and the above input logic of blocks. These data are applied to the diagnosis of a faulty block and line-shorted portion detection.

4. Extraction of the test vector number (TVN) with abnormal I_{DDQ} [6]

The actual measurement procedure shown in the right flow in Figure 1 is presented to extract the TVN with abnormal I_{DDQ}. Leakage current surpassing the allowable maximum value is distinguished as an abnormal I_{DDQ} value. The test vector used to the diagnosis is functional vector applied to the quality selection of LSI circuits, and no special vector to fault detection.Two kinds of leakage state are abnormal state of LSI with penetration current in the normal operation and with multiple faults.

For faulty LSI circuits with penetration current in the normal state, the difference obtained by subtracting the normal penetration current value from the supply current value of a faulty LSI is considered to be the true leakage current. The leakage current of CMOS-LSI is classified generally into two types: normal static state type without penetration current flowing from V_{DD} to GND, and abnormal type with it. The former type of normal value indicates very small fault-free leakage current (under 1uA). Abnormal I_{DDQ} value resulting from physical damage exhibits hundreds to thousands times larger than it does, and hence the TVN with abnormal I_{DDQ} is easily detected by the only faulty LSI, because of the distinctive difference in value between normal and abnormal I_{DDQ}. Recent LSI, represents the latter type, brings the penetration current during normal operation with I/O circuits carrying pull up-down resistors and with inner circuits exhibiting static operational current.

In a LSI with multiple abnormal I_{DDQ} values, using the only relation between TVN and I_{DDQ} value, the total of physical damage's number are incalculable. The leakage current value caused by one fault, however, corresponds to one of these values at least, and hence, for multiple faults, TVNs are classified according to their abnormal I_{DDQ} values and each labeled abnormal value is utilized for the following diagnosis technique.

5. Definition of diagnosis area [7]

Before fault diagnosis, the coordinates of the abnormal portions of each LSI manufacturing process are detected by WIA, following which they are adjusted to the LSI layout coordinates axis. Figure 2 illustrates the definition way of the diagnosis area. The diagnosis area ($2r$ x $2r$) encircling an individual portion located on (x_0,y_0) coordinate is defined in order to compensate for measurement errors with WIA. Circuit elements in the diagnosis area are extracted next using LSI layout data. After this, expected logic states are extracted by logic simulation.

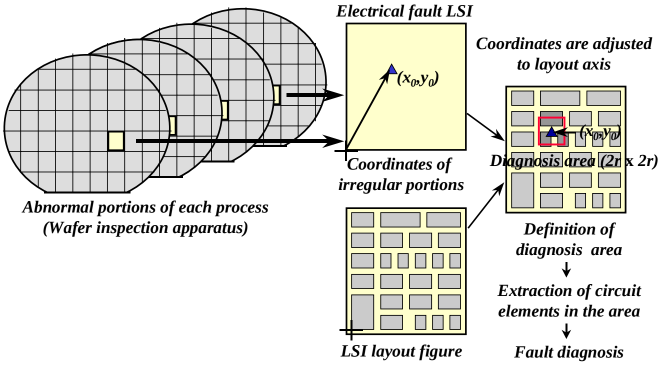


Fig. 2. Defining the diagnosis area.

5.1 Definition of diagnosis area

The maximum *30*um (at *10* x *10* mm^2 chip size) difference between the visual portion, derived by WIA, and the LSI layout coordinate is generated experimentally. To cancel out the difference, a minimum diagnosis area with *30* x *30*um^2 is defined which encircles the coordinates of the visual abnormalities identified with WIA.

5.2 Extraction of blocks in the area

Figure 3 shows the extraction way of the blocks in the diagnosis area. For efficient extraction, a rough area {($2r$+$2Xm$) x ($2r$+$2Ym$)} is defined which encircles the diagnosis area ($2r$ x $2r$) by the maximum block (Xm x Ym) applied to the LSI, and then, the blocks ***(B1, B2, B3, B6, B7, B8, B10)*** with the origin in the rough area are selected. The blocks ***(B2, B3, B6)*** of which a small part at least entered in the initial diagnosis area are extracted finally from the above blocks.

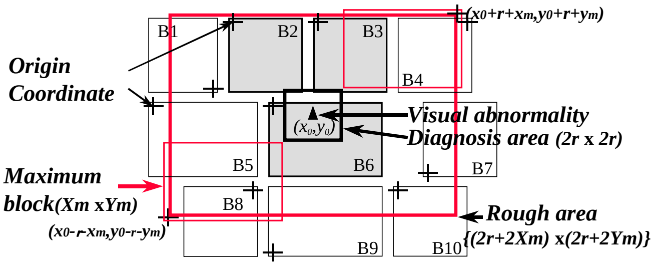


Fig. 3. Extraction way of the blocks in the diagnosis area.

5.3 Extraction of lines in the area

Figure 4 illustrates the extraction way of the lines in the diagnosis area. Lines are divided into the horizontal or vertical segments of each bending point, and these segments make it easy to detect lines in the diagnosis area by the following operation. In the segment selecting operation, every segment above and below this area is eliminated first from all segments and then, the right and left of this area are taken away from the remaining them, shown in Figure 4. Final remaining segments are extracted as the lines in the diagnosis area.

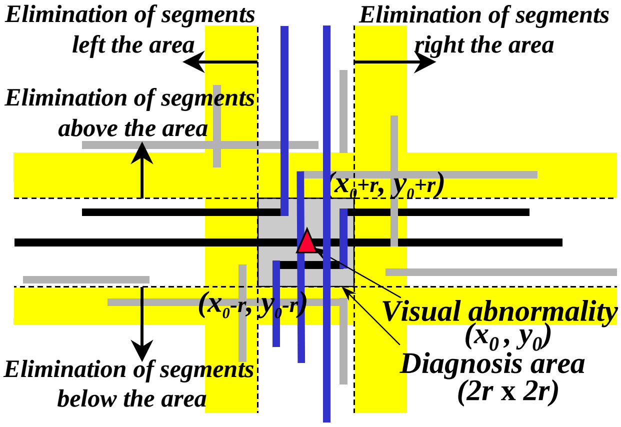


Fig. 4. Extraction way of the segments in the diagnosis area

This diagnosis system has a visual output function to appear the diagnosis area encircling individual portions and the elements in it. Figure 5 illustrates the visual images of diagnosis area with three blocks and thirty lines in true LSI.

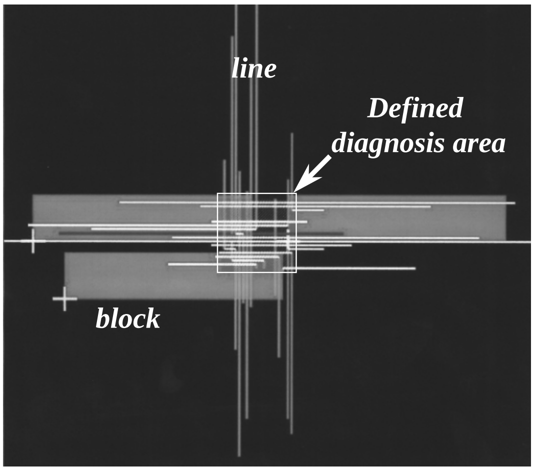


Fig. 5. Illustration of the diagnosis area with three blocks and thirty lines in true LSI.

6. Diagnosis Technique [8][9]

For the fault detection, a diagnosis technique by using the logic state of each element and TVN with abnormal I_{DDQ} is introduced. The basic diagnosis technique employs the comparative operation to determine whether the same logic state with abnormal I_{DDQ} exists in a normal logic state or not. The area with the former element is regarded as a normal area and the latter element is considered to be a suspected faulty area. In this session, the fault block extraction method is first presented and the shorted line extraction way is next introduced.

6.1 Block

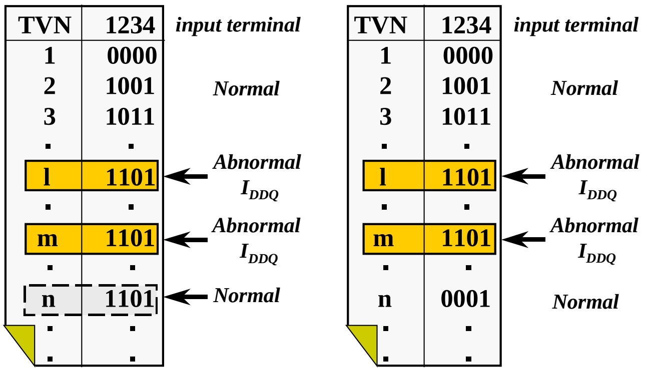
Fundamental algorithm to discern the faulty block is a simple method whether or not the same input logic with abnormal I_{DDQ} exists in the other input combinational logic with normal I_{DDQ}. In this subsection, the discernment of combinational and sequential circuit type is first explained, and then the diagnosis method of each circuit block is described.

The circuit blocks comprising the LSI are classified into two types: combinational and sequential circuit type. The combinational circuit is a simple logic circuit that individual inner logic states are dependent on an arbitrary input logic, and the signal applied to input terminal is transmitted simultaneously to the output terminal. Typical circuit blocks are gates (Inverter, OR, AND, NOR, NAND), multiplexer, adder circuit, and so forth. The sequential circuit is a complex logic circuit that data signal synchronized with clock is held in the inner logic circuit and, after one or several clocks, the operational result appears at the output terminal. The sequential circuit blocks, registered as primitive units, are flip-flop and resistor. Any other large scaled circuit blocks defined by a hierarchical structure are divided into the fundamental combinational and sequential blocks

The above two circuit types have differential diagnosis methods to localize the faulty block, and hence, before fault diagnosis, the circuit type of an investigated block is discerned. Sequential circuit name register file (SRF) which memorizes sequential circuit block text names is utilized to distinguish the block type. The investigated block refers to SRF and whether this block name exists on the SRF is examined. No-existence means that this block is a combinational circuit block and existence means a sequential circuit block.

Figure 6 illustrates the diagnosis method to discern the faulty block of a combinational circuit with unilateral inner logic state depending upon arbitrary input logic. The abnormal I_{DDQ} state appears at TVN ***l*** and ***m*** with input logic (1101). The diagnosis of this block is executed using the comparative operation to see whether the same input logic (1101) with abnormal I_{DDQ} exists in the normal input logic set. Figure 6(a) shows the block that TVN ***n*** with normal state has the same input logic (1101) with abnormal I_{DDQ}, and hence the block is judged to be a normal block. Figure 6(b) denotes the block that the input logic (1101) with abnormal I_{DDQ} does not exist in the normal input logic, and hence the block is considered to a suspected abnormal block.

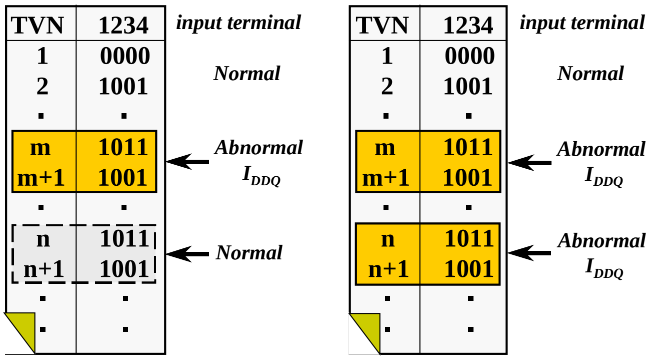
The reason is that an arbitrary input functional logic permits the only inner logic state in combinational circuit, and hence, the input logic being the same as input logic with abnormal I_{DDQ} always brings irregular leakage current. Consequently, the existence of the same input logic with the abnormal I_{DDQ} in the normal state means that the abnormal I_{DDQ} state caused by faulty block seemingly synchronizes with the normal block's input logic, while non existence means that the input logic exhibiting abnormal I_{DDQ} surely causes irregular leakage current.



(a) Normal block (b) Suspected abnormal block

Fig. 6. Illustration of the diagnosis method to discern the faulty block of combinational circuit.

Figure 7 illustrates the diagnosis method to discern the faulty block of a sequential circuit. An abnormal I_{DDQ} state appears at {TVN ***m***, and ***m+1***} with input combinational logic {(1011) and (1001)} respectively. A set of successive input logic with abnormal I_{DDQ} is treated as one group because of the sequential circuit feature. The diagnosis is executed using a comparative operation to see whether the same input combinational logic group {(1011) and (1001)} exist in the normal input logic group. Figure 7(a) shows the block that successive {TVN ***n*** and ***n+1***} with normal state has the same serial input logic {(1011) and (1001)} with abnormal I_{DDQ}, and hence the block is judged to be a normal block. Figure 7 (b) denotes the block that input logic group {(1011) and (1001)} with abnormal I_{DDQ} at {TVN ***m***, and ***m+1*** } and {TVN ***n*** and ***n+1*** } does not exist in the normal input logic set, and hence the block is considered to a suspected abnormal block.



(a) Normal block (b) Suspected abnormal block

Fig. 7. Illustration of the diagnosis method to discern the faulty block of sequential circuit.

The reason is similar to it of combinational circuits. Arbitrary input combinational logic group of sequential circuit block allows the specific inner logic state, and thereby the input combinational logic group which is the same as logic group with abnormal I_{DDQ} always causes irregular leakage current.

6.2 Shorted line diagnosis

To diagnose circuit portions with shorted signal lines, the logic value of each element in the diagnosis area is employed. Three cases in the diagnosis area are the shorted-line between inside lines of block, lines, and inside line of block and line.

An investigation of shorted-line in block is executed simultaneously during the above block diagnosis.

The diagnosis method of shorted-line between lines is presented. All lines in the diagnosis area is regarded as one group and the shorted line detection is carried out to the combinational logic in it. The diagnosis technique is the same as combinational circuit. TVN with normal state has the same logic with abnormal I_{DDQ}, and hence the line group is judged to a normal line group. The logic with abnormal I_{DDQ} does not exist in the normal state, and hence the line group is considered to a suspected abnormal line group with shorted-line.

The diagnosis way of shorted-line fault between inside line of block and line is presented. For the inner logic state of block, the input logic state of it is substituted. The reason is that the arbitrary input logic state sets up an individual inner logic state. The diagnosis is executed by the logic table combing the input logic of each block and the logic value of all line. The diagnosis is executed by the comparative operation to see whether one or more of the same logic with abnormal I_{DDQ} exist in the normal logic set. TVN with normal state has the same with abnormal I_{DDQ}, and hence this combination group is judged to be a normal group. The same logic with abnormal I_{DDQ} does not exist in the normal state, and hence the group is considered to a suspected abnormal group with shorted-line. The diagnosis method is dependent on the block type. In the above explanation with combinational circuit block, the diagnosis way of the set elements complies with the same it of combinational block. In the case of sequential circuit block, the diagnosis technique of the set elements applies, however, it of sequential block.

6.3 Assessing of visual abnormality

The presence of a fault element in the diagnosis area indicates that the visual abnormality identified with WIA has grown into a fatal defect.

7. Experimental results

7.1 Example 1

This technology was applied to determine a killer defect from the visual abnormalities of an actual faulty LSI with abnormal I_{DDQ}. The sample was a 650,000-gate CMOS-logic LSI with a 0.35um design rule, and had three metal layers and a hierarchical circuit structure (maximum depth: 10 layers) with 32,000 test vectors. First, the hierarchical circuit was divided into 72,011 functional blocks (minimum size: one gate, maximum size: twenty-eight gates, average size: nine gates), and then, the expected input logic of each block and logic state of every line were extracted by net list, test vector, and logic simulation. After a strobe time of 800 ns was decided, the relation between TVN and I_{DDQ} value was examined using a LSI tester. Figure 8 shows the measurement result with 0.2mA abnormal I_{DDQ} value.

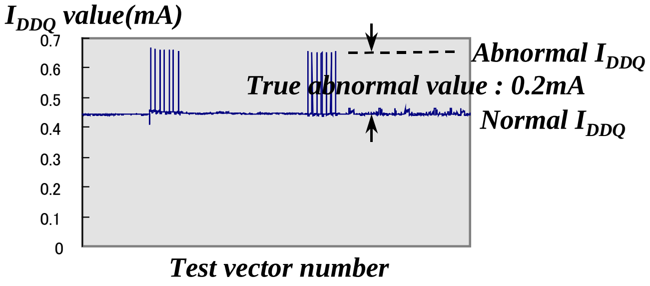
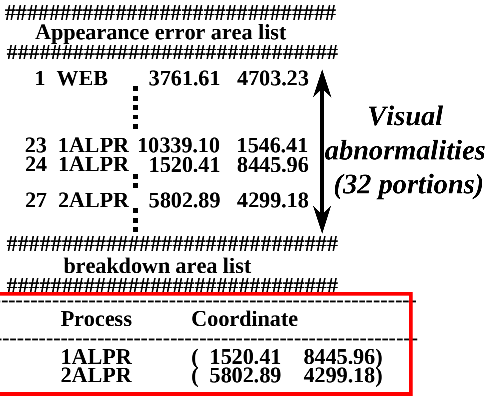


Fig. 8. Test vector number vs. abnormal I_{DDQ} value.

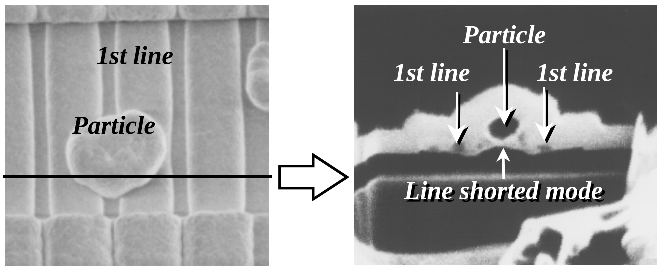
Thirty-two visual irregular portions in this LSI were detected by WIA. After diagnosis areas with *60* x *60* um^2 surrounding each abnormality were defined, the circuit elements (the mean number of blocks: 1.7 blocks, the mean number of lines: nine lines + two power source lines) in each area were diagnosed using the above fault detection method. The diagnosis result revealed two probable killer portions shown in Table 1. Appearance error area list (AEAL) in it illustrates thirty-two visual abnormalities denoting serial number, detected manufacturing process name, and coordinates in order, and Breakdown area list (BAL) indicates two probable killer portions (No. 24 and No. 27) showing the same. Their abnormalities were particles with *3.5* x *1.5* um^2 at 1ALPR (*1st line Photo-Resist*) process and *3.2* x *0.8* um^2 at 2ALPR (*2nd line Photo-Resist*) process respectively.

Table 1. Diagnosis results



```
################################
  Appearance error area list
################################
   1  WEB      3761.61   4703.23
                 :
  23  1ALPR   10339.10   1546.41
  24  1ALPR    1520.41   8445.96
                 :
  27  2ALPR    5802.89   4299.18
                 :
################################
     breakdown area list
################################
-----------------------------------------
  No.      Process      Coordinate
-----------------------------------------
  24       1ALPR        ( 1520.41   8445.96)
  27       2ALPR        ( 5802.89   4299.18)
```

Physical analysis was executed. The observation by SEM (Scanning Electron Microscopy) indicated a particle between the first metal line at No. 24 portion and the cross sectional analysis by FIB (Focused Ion Beam) pointed out the line-shorted portion, shown in Figure 9. No. 27 could not detect, however, the fault. The abnormal I_{DDQ} state caused by No.24 portion seemingly synchronized with No.27 input logic. The cause of the false faulty element extraction cannot be explained generally because this detection largely depends on the structure of each circuit. The diagnosis times after preparing the element data extraction was less than two minutes per one portion. The obtained defect information was fed back to manufacturing processes.



SEM image of abnormality

Cross section by FIB defabrication

Fig. 9. Physical analysis indicated a bridge-fault between the line, resulting from metal Particle (No.24)

7.2 Example 2

Next example is the diagnosis result of four pieces of process monitoring LSI with abnormal I_{DDQ} by the above technique. Figure 10 shows the diagnosis result and verification images of abnormal photon with Photo-emission microscopy. The result indicated that abnormal illuminated portions were detected on the diagnosis area, encircling the visual abnormal portions. In the Figure 10, left-side description means that wafer number- chip portion (x-y), process name of abnormality detection, coordinates of the portion, fault block name, and abnormal I_{DDQ} value in order.

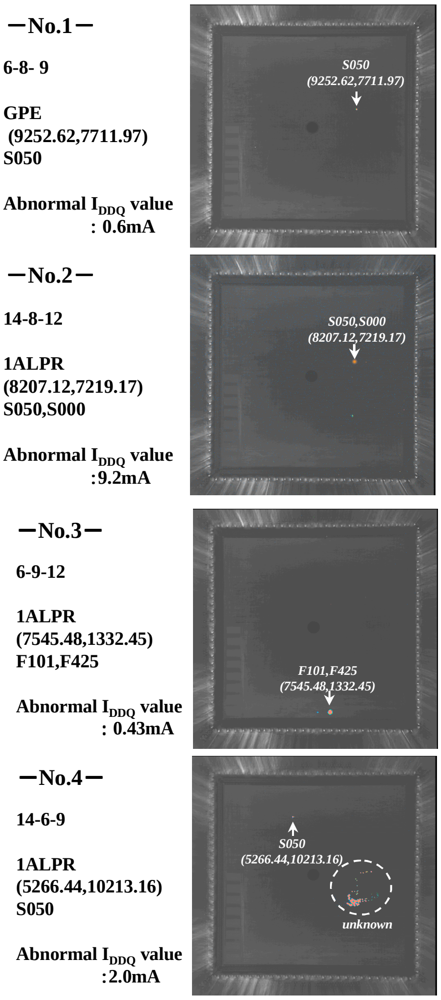


Fig. 10. The diagnosis result and verification images

8. Conclusions

Actual faulty LSI circuits with abnormal I_{DDQ} is brought by ordinary outbreaks and common physical damage. Using this phenomenon, I developed a CAD-based fault diagnosis technique to detect the killer defects in several abnormalities identified by WIA. The technique includes a way to separate various leakage faults and a technique to define the diagnosis area encircling the abnormal portions. This method identifies faulty blocks and circuit portions with shorted signal lines, making it possible to cover most physical damages. The obtained killer defect information could be fed back to logic LSI manufacturing processes, helping to improve the manufacturing yield. The diagnosis time was under two minutes per one portion, and parallel diagnosis operations for several abnormalities drastically shortened its times. As a result, I conclude that this diagnosis technique is an indispensable tool to manage the yield of logic LSI circuits.

Acknowledgments

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