Built - In Self Test insertion in a System On a Chip

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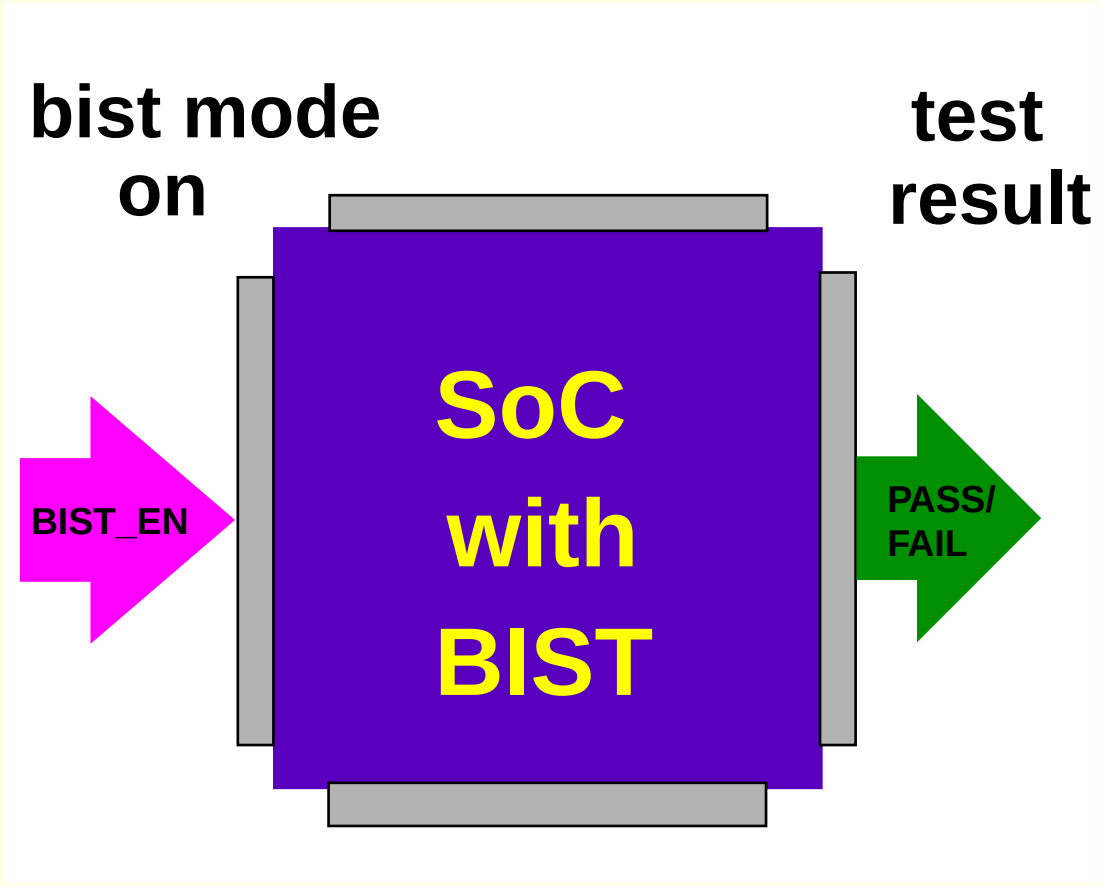


- added test circuitry carries out the test and gives the final pass/fail result,
- to achieve the best fault coverage circuitry specific test vectors are in use

DESIGN DESCRIPTION - SYSTEM ON A CHIP FOR TELECOMMUNICATIONS PURPOSES

200k gates DECT basestation

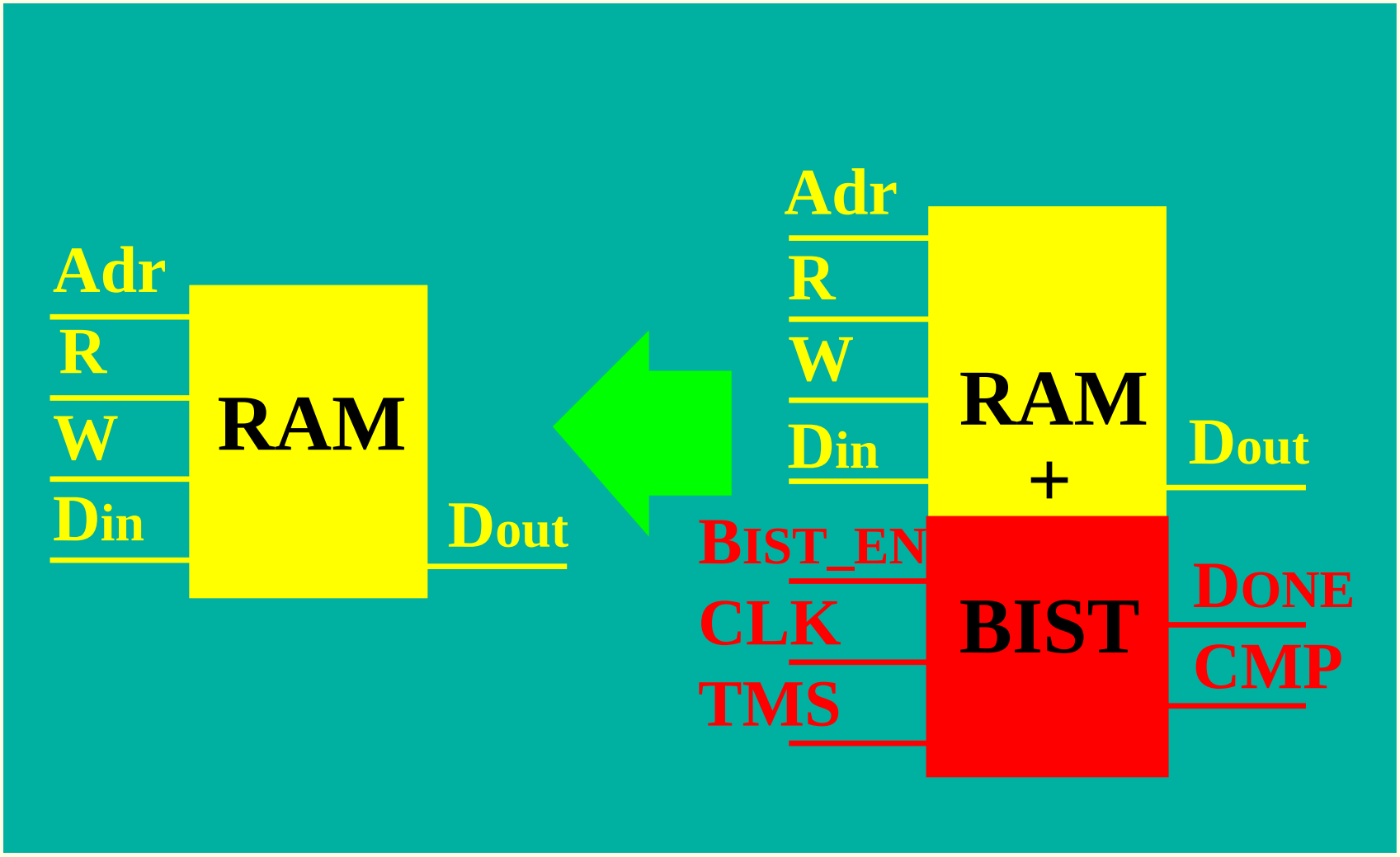
ARM subsystem

DFT: scan test, IDDQ, boundary scan, ARM test, nand tree test, BIST

RAMs on board:

1 x 5120 words, 8 bit RAM
5 x 2048 words, 8 bit RAMs
4 x 64 words, 8 bit RAMs
1 x 64 words, 8 bit 2 port RAM
1 x 64 words, 9 bit 2 port RAM

BIST'ed MEMORY REPLACES RAM



BIST - PROS AND CONS

ADVANTAGES

- high fault coverage
- test mode can be switched on whenever it is necessary
- shorter test times - memories can be tested in parallel
- reusability, repeatability
- embedded RAMs with no direct access to pins can be tested
- lower cost of the test

DISADVANTAGES

- silicon area overhead
- extra pins or multiple pins required
- memory access time - extra steering logic

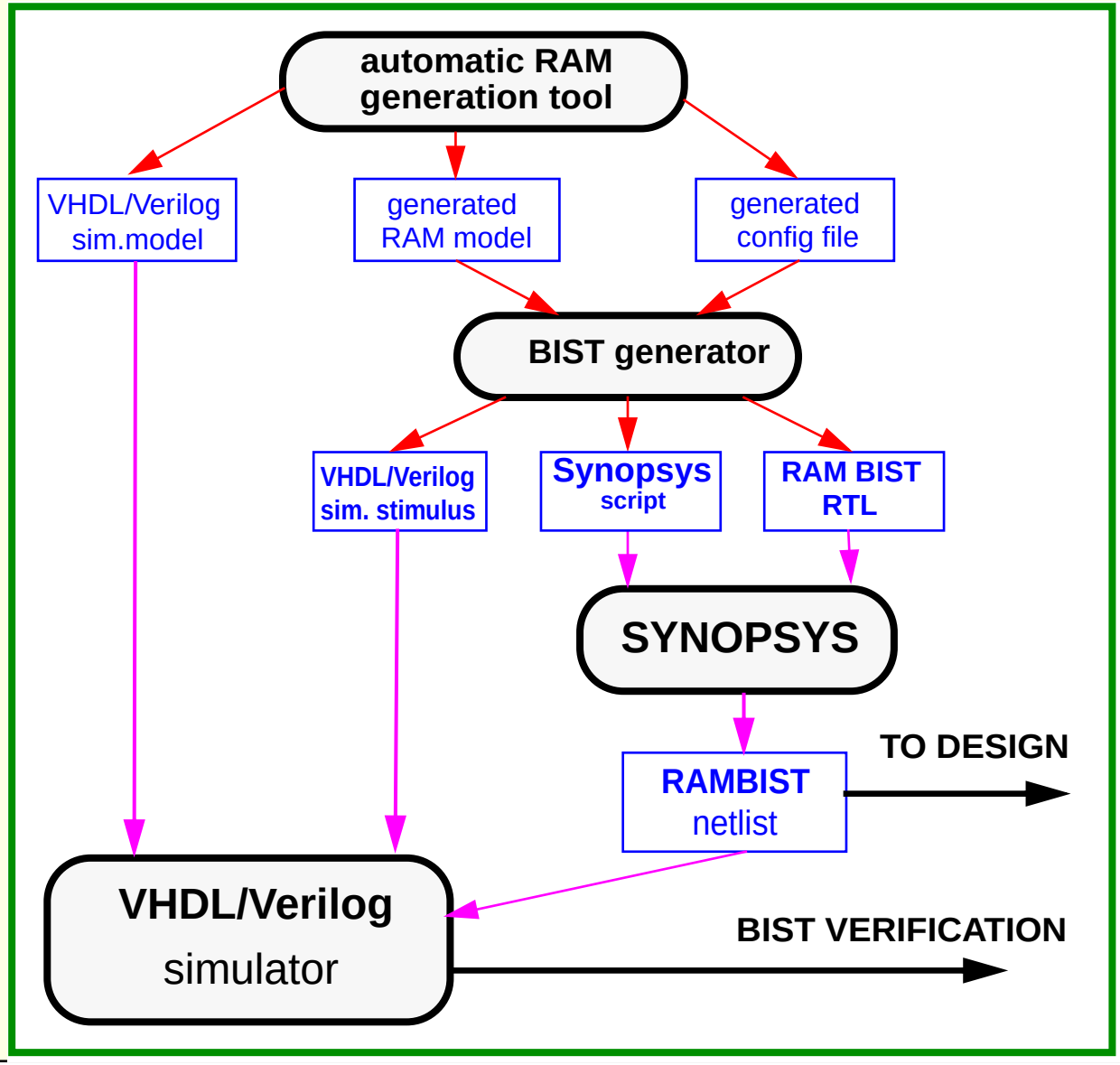
BIST RELATED SUPPLIES from MEMORY CORE PROVIDER

RAM VHDL
models
synthesis scripts

Simulation files
bist_testbench.vhd
_collar_config_syn.vhd
bist_config.vhd

BIST package - RTL
RAMtype_bist_collar.vhd
bist_cntrl.vhd
bist_assembly.vhd
bist_testbench.vhd

BIST INSERTION - DESIGN FLOW



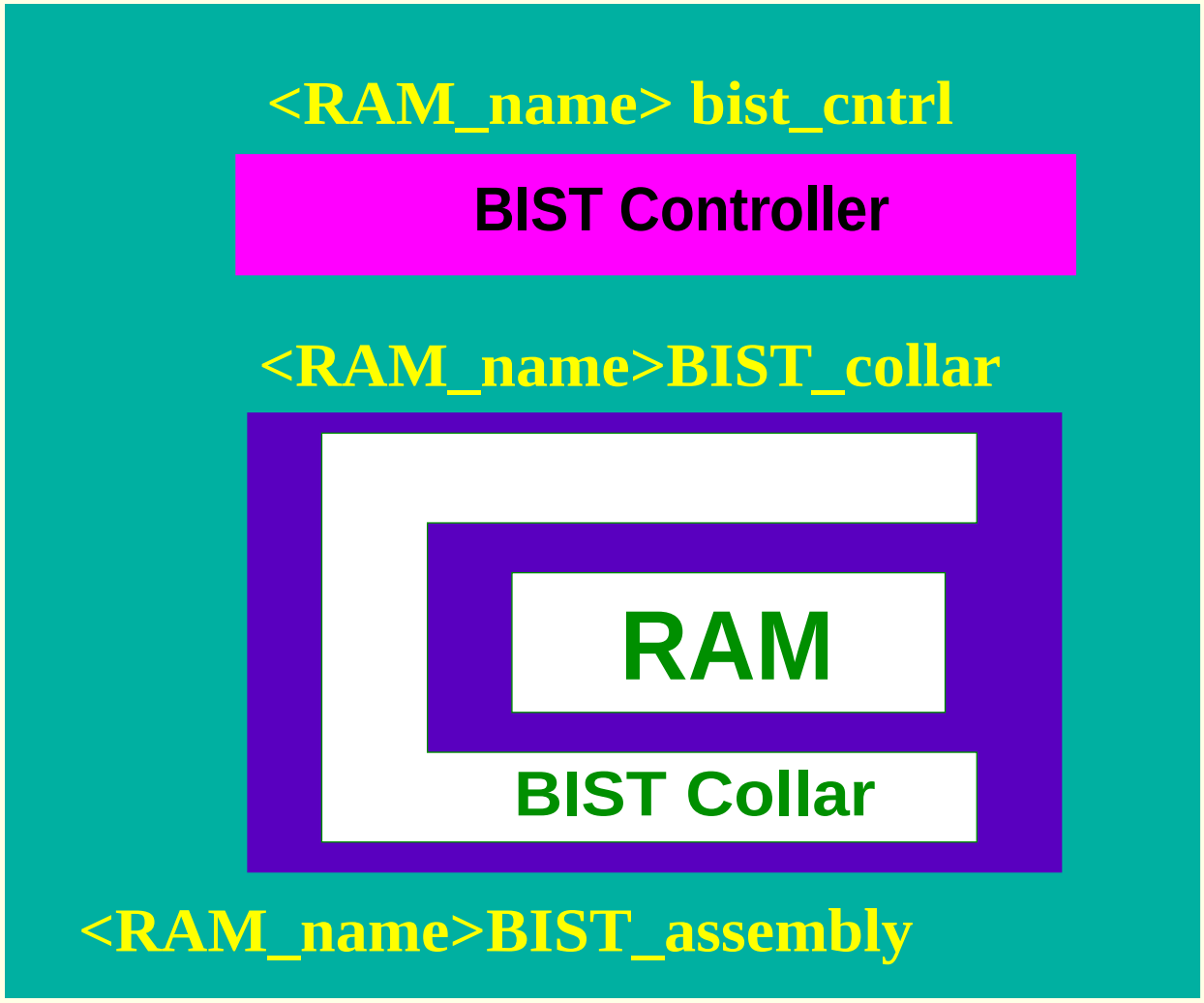
BIST VERIFICATION

The goal of verification is to check if the Synopsys synthesized RAM BIST circuitry operates with the RAM properly. This was done with generated RAM simulation model

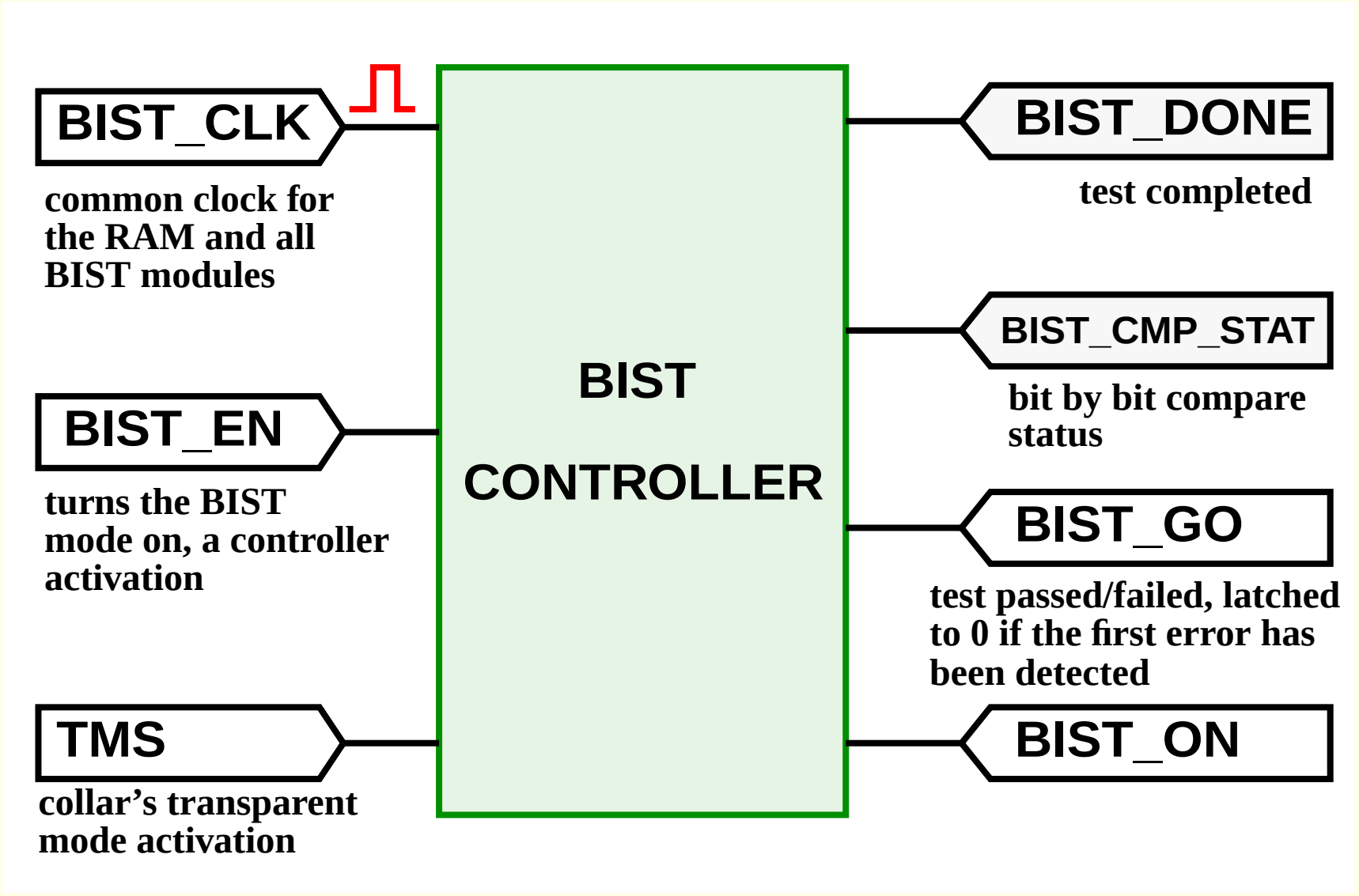
During verification BIST - generated testbenches were used to simulate RAM BIST circuitry

The testbench enables BIST mode and monitors status signals

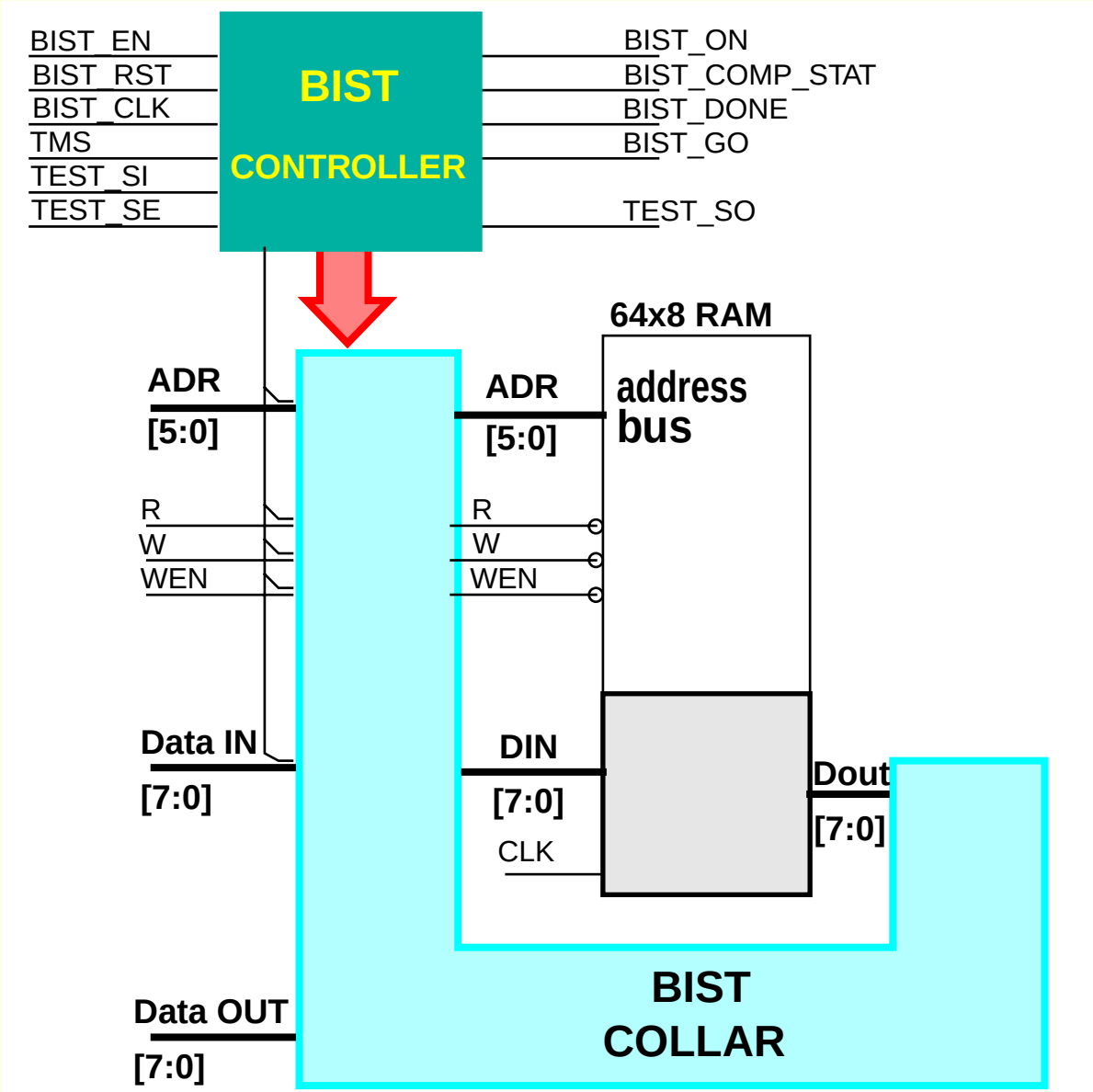
BIST HIERARCHY



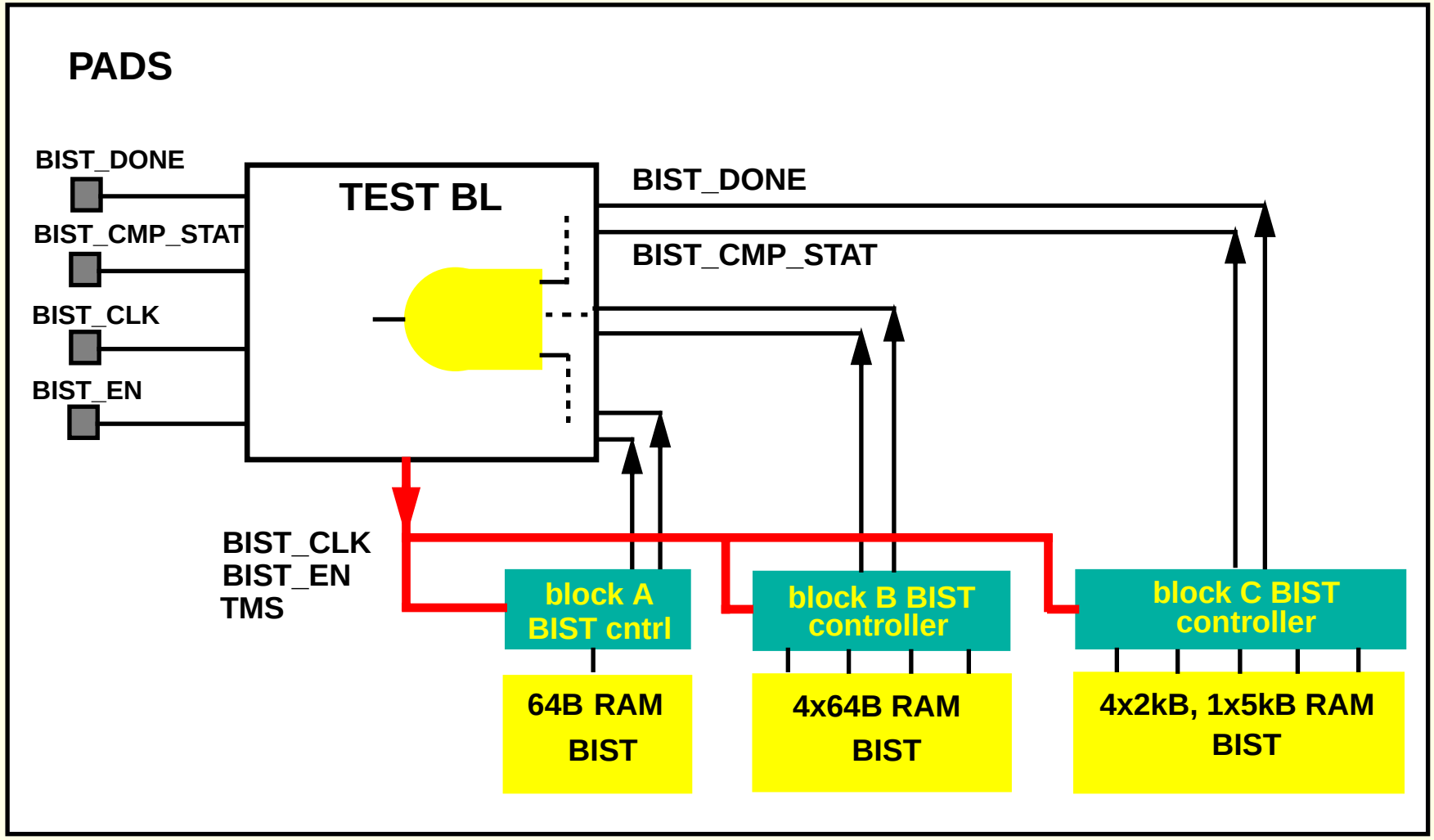
BIST PINS AND SIGNALS



RAM WITH BIST CIRCUITRY



TOP LEVEL BIST CONNECTIONS



PIN REQUIREMENTS

4 BIST SIGNALS ARE REQUIRED TO BE ACCESSIBLE DIRECTLY FROM PINS

- **BIST_CLK,**
- **BIST_EN,**
- **BIST_DONE,**
- **BIST_CMP_STAT**

PINS WHICH CAN NEVER BE USED FOR BIST SIGNALS

- **ASYNCHRONOUS RESET,**
- **DEDICATED TAP CONTROLLER PINS**
- **BIDIRECTIONAL AND OUTPUT PINS WITH CRITICAL TIMING NOT ACCEPTING ADDITIONAL MUX DELAY**

TEST ALGORITHM -the deterministic SMARCH algorithm was implemented

The algorithm consisted of the following steps:

$$(R_{0/1\text{-}0}W_{1\text{-}0});\ (R_{1\text{-}0}W_{0\text{-}0});\ \Uparrow(W_0);\ \Uparrow(R_0W_1)\ \Uparrow(R_1W_0);$$

$$\Downarrow(R_0W_1);\ \Downarrow(R_1W_0);\ \Downarrow R_0$$

The following types of faults are being detected:

- Stuck-at faults (SAF),
- Coupling faults - shorts between cells, static coupling,
- Multi Access faults - shorts between address/data lines,
- Transition faults,
- Data Retention faults.

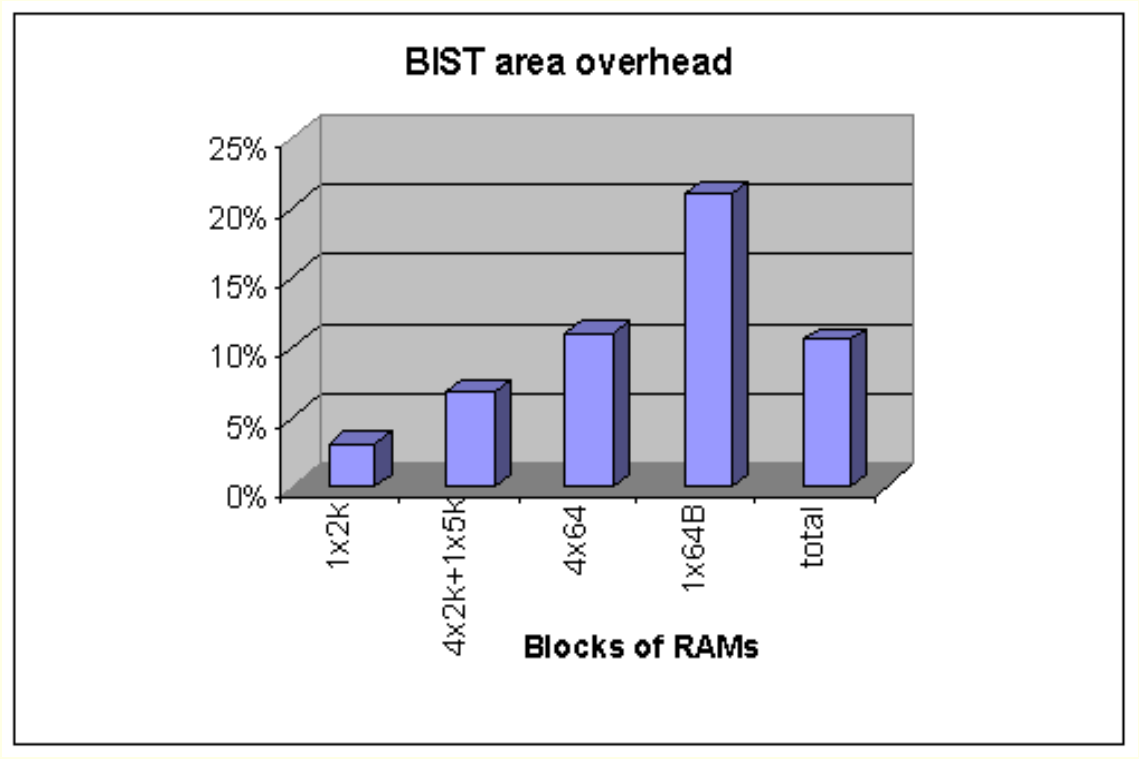
PROBLEMS ENCOUNTERED

- collar functionality - no multiplexers for BIST_CLK going to RAM during the test,
- all the data to the RAM's in BIST mode was set up by the BIST controller on the rising edge of BIST_CLK
- bugs in automatically generated wrappers

MEMORY TEST TIME

Block of RAM	1 x 64B	1 x 2kB	4x2kB, 1x5kB
TEST TIME clock cycles	5930	188458	1224898

BIST AREA OVERHEAD



CONCLUSION

- **BIST - an efficient tool to test RAMs,**
- **reduces test time and costs,**
- **tests can be done during the operational life of a chip,**
- **suitable for SoC - in designs where there is no direct access to pins,**
- **BIST was implemented by replacing RAMs with BIST'ed memories,**
- **BIST area overhead was 10.5% which is acceptable,**
- **delay caused by additional MUXes is not significant**

THANK YOU