Application of Deterministic Logic BIST on Industrial Circuits

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Abstract

We present the application of a deterministic logic BIST scheme on state-of-the-art industrial circuits. Experimental results show that complete fault coverage can be achieved for industrial circuits up to 100K gates with 10,000 test patterns, at a total area cost for BIST hardware of typically 5%-15%. It is demonstrated that a trade-off is possible between test quality, test time, and silicon area for the BIST hardware. In contrast to BIST schemes based on test point insertion no modifications of the circuit under test are required, complete fault efficiency is guaranteed, and the impact on the design process is minimized.

1. Introduction

Modern IC design technologies and the introduction of systems-on-chip (SOC) using embedded cores allow to integrate more and more gates on a single IC. To test such large ICs, a huge amount of test patterns is required. In addition, these large ICs show a sharp increase in the ratio of number of gates per pin. Transporting lots of test data over a limited amount of IC pins is causing a bandwith problem, which leads to increasing test time and the use of expensive test equipment. Built-in self-test (BIST) is becoming an attractive alternative, since it solves the bandwith problem by eliminating the need for external testing [Zori99].

For industrial applications, logic BIST synthesis is currently supported by a few commercially available CAD tools [MNBB98, HETH99] based on the STUMPS architecture [BaMc84] for pseudo-random testing. Test patterns are generated and responses are compressed using linear feedback shift registers (LFSRs) (see Figure 1). If a single LFSR is used to generate bit sequences for multiple scan chains, these bit sequences may only differ by a small number of shifts and as a result, the fault coverage may be reduced [BMS87, Bard92]. For this reason, phase shifters [BaMc86, Bard90, RTT98, HETH99] are inserted between the LFSR and the scan chains in order to generate decorrelated pseudo-random patterns. However, even decorrelated pseudo-random patterns cannot guarantee complete fault coverage.

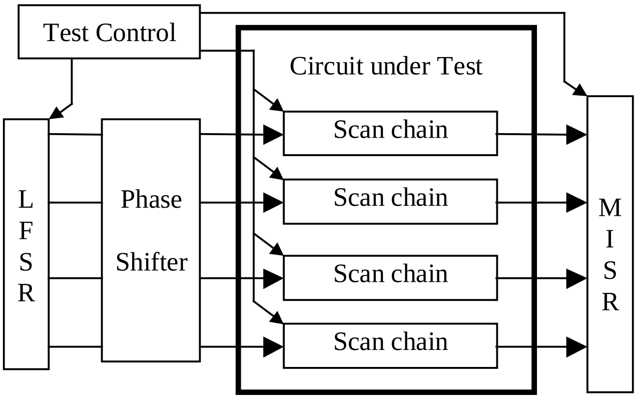

Figure 1: STUMPS scheme with phase shifting logic

The fault coverage can be improved by using an enhanced BIST scheme and/or by applying additional external test patterns. Commercial logic BIST tools currently offer test point insertion into the CUT to improve its pseudo-random testability [HaFr74, STS91, TaRa96]. Test point insertion however implies modifications of the CUT. This requires additional silicon area and it may also have a negative impact on the timing behavior if test points are inserted in critical paths. Timing verification after test point insertion is therefore required as an additional task in the design process, and further design iterations may be required to solve timing violations. Furthermore, even test point insertion cannot guarantee complete fault coverage. For instance, 95-96% stuck-at fault coverage has been reported in [HETH99] for the practical application of logic BIST with test point insertion on large industrial circuits (200-800K gates).

A straightforward approach to achieve complete fault coverage is to apply external test patterns – which have been generated by ATPG tools – to the CUT using traditional scan testing, in addition to the pseudo-random patterns. However, this approach still requires a considerable amount of external testing. In [BASS89] it has been reported that detecting the last 10% of undetected faults typically requires 70% or more of the test patterns in an ATPG test set. In [HETH99], external test patterns were applied on top of the BIST scheme with test points for improving the fault coverage from 95-96% to 96-97%, which still required 25-65% of the patterns in the full ATPG test set.

Complete fault coverage without CUT modifications and external test patterns can be achieved by using a BIST scheme containing a more sophisticated pattern generator. Examples of this approach are weighted random pattern generators [Wund87, BRGL89, StWu91], pseudo-exhaustive pattern generators [Aker85, HWH90], and deterministic pattern generators [HRTW95, ToMc96, WuKi96, KiWu97, KiWu98, KiWu99]. However, the price for obtaining complete fault coverage usually is a relatively large amount of additional silicon area for the sophisticated pattern generator.

In [KiWu97, KiWu98] a deterministic logic BIST scheme has been presented, which is more efficient than pseudo-random BIST in terms of silicon area and fault coverage for the ISCAS'85 and ISCAS'89 benchmark circuits [BrFu85, BBK89]. The basic principle of this BIST scheme is that the sequence of pseudo-random test patterns is modified by embedding deterministic patterns into the sequence. The target structure of the deterministic logic BIST scheme is shown in Figure 2. The pattern generator consists of an LFSR and a small combinational function, the sequence-generating logic (SGL). The SGL passes the bit sequences generated by the LFSR to the scan chains, and modifies these sequences at certain bit positions which are selected by both the state of the test control unit and the state of the LFSR. These sequence modifications provide that additional deterministic patterns are generated and complete fault coverage can be guaranteed.

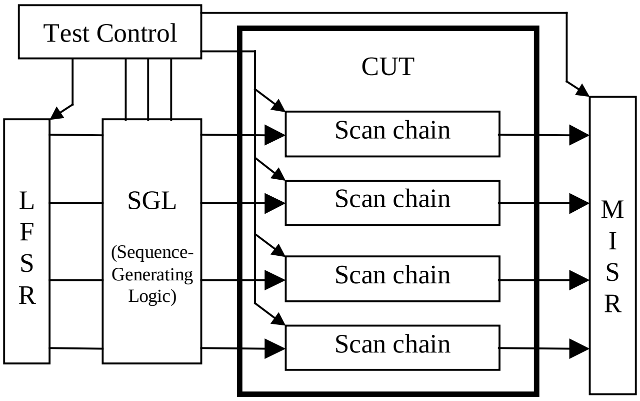

Figure 2: Target Structure of the deterministic BIST scheme

In the present paper we describe the application of this deterministic BIST scheme on industrial designs which differ considerably from the ISCAS benchmark circuits. First the deterministic BIST scheme and the BIST synthesis algorithm are summarized in Section 2. The designs that were investigated together with the DfT measures and preparations for the BIST synthesis are discussed in Section 3. Finally, experimental results are presented in Section 4.

2. BIST synthesis algorithm

The synthesis algorithm for the sequence-generating logic (SGL) is described in [KiWu98] and [WuKi96]. For a better understanding of the rest of the paper, a brief summary follows.

The SGL modifies the pseudo-random test patterns generated by the LFSR in such a way that deterministic patterns are embedded. The structure of the SGL is shown in Figure 3. It consists of XOR gates and a bit-flipping function (BFF). The current state of the LFSR as well as the bit counter and the pattern counter of the test control unit serve as inputs for the BFF.

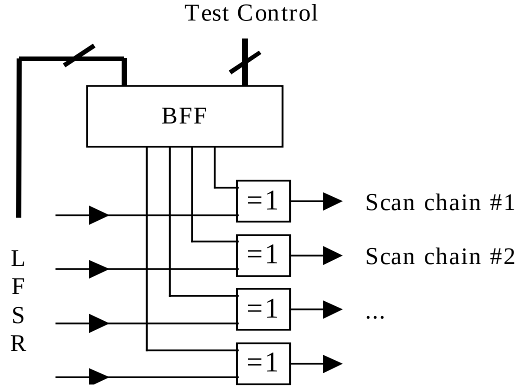

Figure 3: Sequence-Generating Logic

In a pseudo-random test set only a few bits are really necessary for detecting faults, and furthermore, deterministic patterns can easily be embedded by modifying just a very small number of bits [WuKi96]. This allows that the BFF can be minimized very efficiently. Furthermore, since the outputs of the pattern generator also depend on the current state of the test control unit, the LFSR may be very small. This does not only reduce the chip area of the LFSR, but also the BFF may be smaller as the autocorrelation of deterministic test patterns can be exploited [KiWu97]. Furthermore, the BFF can overcome dependencies between different LFSR outputs, so no phase shifting is required [KiWu98].

The BFF is constructed by means of an iterative algorithm as sketched in Figure 4. The algorithm starts with an empty BFF (resulting in no pattern modifications yet) and terminates when sufficient fault coverage is achieved. In each iteration, the BFF is enhanced, so that new deterministic patterns are produced while certain old patterns, which are essential for detecting faults that are already detected, remain unchanged.

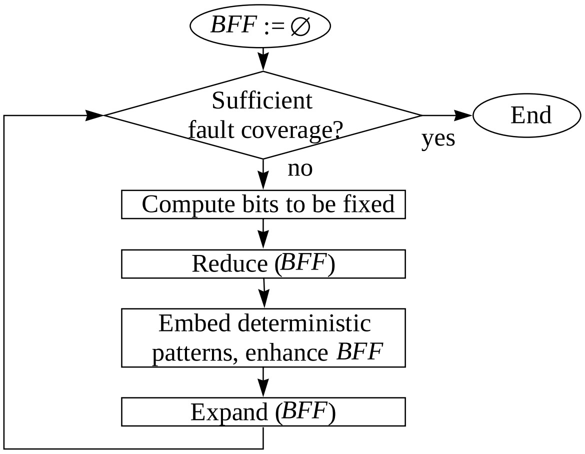
BFF := ∅
Sufficient fault coverage?
yes
End
no
Compute bits to be fixed
Reduce (BFF)
Embed deterministic patterns, enhance BFF
Expand (BFF)

Figure 4: BFF synthesis algorithm

Pattern bits not to be changed are determined by three-valued fault simulation. The states of the LFSR and the test control unit which correspond to these essential bits, specify inputs for the BFF for which its function must not change. The set of states corresponding to the essential bits of the *i*-th scan chain is called the *i*-th fix-set FIX_i.

An automatic test pattern generator (ATPG) is used to generate deterministic patterns for all the currently undetected faults. In order to obtain a small BFF, the ATPG tool should minimize the number of specified bits, e.g. as described in [HRTW95]. For one or several of these patterns a currently generated pattern with a minimum number of conflicting bits is selected. A mapping of a deterministic pattern *d* to a currently generated pattern *r* is characterized by two state sets per scan chain. For each chain *i* the set $ON_i(d, r)$ corresponds to the bits that have to be changed, and $OFF_i(d, r)$ corresponds to the bits that must not be changed. The BFF is modified such that its output changes for all states specified by $ON_i(d, r)$ but for none of the states specified by FIX_i and $OFF_i(d, r)$.

In order to achieve an efficient implementation of the BFF, the ESPRESSO-like logic minimization procedures "Expand" and "Reduce" [BHMS84] are integrated into the main loop of the algorithm. All the states not contained in any of the sets FIX_i, $ON_i(d, r)$ or $OFF_i(d, r)$ specify “don't care” conditions which can be exploited efficiently for the minimization.

3. Circuits under investigation

In general, industrial circuits differ considerably from the ISCAS'85 and ISCAS'89 [BrFu85, BBK89] benchmark circuits. The ISCAS circuits are older designs originating from the 1980's, and they are relatively small: there are only 5 circuits that have more than 10,000 signal lines and the largest circuit (s38584) contains 38,584 signal lines. Furthermore, the ISCAS circuits contain logic gates only and they do not include bus structures, embedded memories, mixed-signal modules, and multiple clock domains as typically found in industrial circuits.

We applied the deterministic logic BIST scheme on 26 state-of-the-art industrial circuits from various application fields. These industrial circuits are modules extracted from various Philips designs, including an 8-bit microcontroller, a programmable DSP, and various dedicated ICs for video processing, audio processing, graphics processing, and telecommunication. All circuits have been proven on silicon. They are all full-scan designs with muxed-scan flipflops configured in multiple scan chains, and most larger circuits contain embedded memories and multiple clock domains.

Table 1 shows the complexity of the circuits in terms of number of NAND-equivalent gates (i.e. circuit area divided by the area for a 2-input NAND gate), flipflops (FF), primary inputs (PI), and primary outputs (PO). In general, these industrial circuits are larger than the ISCAS circuits. The two rightmost columns FC_{rand} and FE_{rand} show the fault coverage (i.e. number of detected faults with respect to all faults) and the fault efficiency (i.e. number of detected faults with respect to non-redundant faults) that is obtained using 10,000 pseudo-random patterns.

circuit	#gates	#FF	#PI	#PO	FC_{rand}	FE_{rand}
p2221	2,208	217	69	19	79.29%	81.88%
p2441	2,270	183	68	95	83.99%	85.94%
p2675	1,788	108	274	128	99.45%	99.54%
p4207	3,580	183	12	81	96.23%	96.57%
p4210	4,218	305	62	52	94.46%	94.47%
p5918	4,444	201	107	49	95.18%	96.53%
p6291	5,976	382	85	39	96.04%	96.80%
p7318	8,832	1,345	8	15	99.37%	99.84%
p7890	6,771	381	64	77	98.62%	98.95%
p9041	10,246	369	289	33	96.97%	97.00%
p10705	10,355	635	123	120	95.15%	95.35%
p12292	9,957	365	203	67	96.72%	97.21%
p13033	12,314	711	251	92	95.11%	95.57%
p13651	11,434	582	134	38	97.50%	99.84%
p14473	12,356	690	194	446	85.52%	86.39%
p17828	19,323	1,731	124	134	95.88%	96.82%
p22383	25,834	966	631	144	92.85%	92.99%
p23572	28,692	1,369	131	145	80.50%	85.53%
p24370	20,448	683	325	164	93.08%	94.40%
p25015	22,848	1,466	381	69	93.89%	98.30%
p27530	20,089	400	159	65	98.14%	98.23%
p44177	49,073	3,644	72	71	96.17%	97.25%
p52251	54,914	4,676	144	252	98.92%	99.32%
p52922	69,986	3,922	179	2,486	89.81%	92.66%
p64984	63,508	5,593	53	49	93.20%	94.07%
p80590	92,319	2,675	1,025	159	98.68%	99.09%

Table 1: Circuit characteristics

In order to prepare the circuits for logic BIST, we made the following modifications to the circuits:

a) We provided that a single clock is used in multiple clocks circuits when the BIST logic is active.

b) We modified the embedded memories either by adding a scan chain around these embedded memories or by adding bypass logic. The scan chain provides that all memory inputs and outputs can be controlled and observed by flipflops. The bypass logic connects the memory inputs directly to the memory outputs by means of multiplexers and XOR-gates in test mode.

c) We added a scan chain around the circuit, which allows all primary inputs to be controlled from the LFSR and all primary outputs to propagate into the MISR.

These circuit modifications provide that no unknown values are generated in the circuit. This is an essential requirement for BIST, since unknown values that propagate into the MISR may corrupt the signature. We assumed that the circuit modifications did not corrupt the timing behavior, but we did not verify this assumption. Modifications b) and c) are required for any logic BIST scheme, while modification a) is not necessary in our deterministic BIST scheme if a controller is used as described in [NBH94] or [HETH99].

4. Experimental results

4.1 Experimental setup

In the experiments, we applied 10,000 pseudo-random test patterns. Our target was to apply deterministic logic BIST and achieve 100% fault efficiency (i.e. all non-redundant faults will be detected). During the experiments, we varied parameters as the LFSR size and the LFSR polynomial. For silicon area estimation, we synthesized the circuits using a Philips 0.25 µm CMOS technology library.

4.2 Fault coverage and fault efficiency

When applying deterministic logic BIST, 100% fault efficiency was obtained for 12 out of the 26 circuits. For the remaining 14 circuits we obtained a fault efficiency >99.9%. The reason for not achieving 100% fault efficiency in all cases is that the academic ATPG tool aborted on some faults. Hence, not reaching 100% fault efficiency is purely due to tool limitations and not at all a limitation of the method. Since the number of aborted faults is less than 0.1% in all cases, their impact on the synthesis results reported below can be considered neglectable.

4.3 Deterministic test patterns

The efficiency of the deterministic BIST scheme strongly depends on the number of specified bits in deterministic patterns. Table 2 provides figures on the deterministic patterns for the industrial circuits: the number of embedded deterministic patterns (#det. pats), the number of pseudo-primary inputs (#PPI), and the maximum number (#spec. bits max.), the minimum number (#spec. bits min.), and the average number (#spec. bits aver.) of specified bits in the embedded deterministic patterns.

circuit	#det. pats	#PPI	# spec. bits max.	#spec. bits min.	#spec. bits aver.
p2221	61	286	25	14	20.4
p2441	48	251	30	11	23.8
p2675	3	382	14	8	10.0
p4207	86	195	35	12	18.3
p4210	61	367	122	49	68.8
p5918	61	308	25	16	21.0
p6291	128	467	109	9	49.6
p7318	4	1,353	12	8	10.3
p7890	43	445	36	17	24.7
p9041	139	658	58	19	37.7
p10705	179	758	35	11	22.7
p12292	173	568	78	16	38.4
p13033	275	962	47	12	22.6
p13651	3	716	39	32	36.3
p14473	595	884	111	14	40.8
p17828	289	1,855	31	11	19.9
p22383	654	1,597	79	13	39.2
p23572	1,025	1,500	35	12	20.9
p24370	595	1,008	103	13	32.5
p25015	190	1,847	79	12	27.1
p27530	309	559	93	16	41.1
p44177	681	3,716	55	10	18.4
p52251	135	4,813	28	11	17.1
p52922	995	4,101	80	4	36.7
p64984	2,142	5,646	364	7	27.8
p80590	356	3,700	51	13	30.2

Table 2: Embedded deterministic patterns

Table 2 indicates that the number of specified bits is quite small and does not generally increase with the size of the circuit or the number of pseudo-primary inputs. A similar observation has been reported with the ISCAS'85 and ISCAS'89 benchmark circuits in [HRTW95]. For circuits which require a relatively large maximum number of specified bits (e.g. p14473 and p64984), only few patterns actually require this maximum number. Hence, a good encodability of deterministic patterns can be expected even for circuits larger than those presented in this paper.

4.4 Silicon area

The synthesis results are shown in Table 3. The numbers are estimates of the actual silicon area since they only include the area for logic gates while leaving out the area for wiring as well as the area for embedded memories. Table 3 shows the total silicon area for the scannable circuit (core area), the percentage of silicon area required for making the circuit fully scannable (scan area), and the percentage of silicon area required for the complete BIST hardware (BIST area). The silicon area for the BIST hardware is the sum of the silicon area for the LFSR, MISR, test controller, and the sequence-generating logic (SGL).

circuit	core area (µm^2)	scan area	BIST area		
			total	LFSRs & test control	SGL
p2221	59,607	16.38%	26.91%	17.41%	9.50%
p2441	61,281	13.44%	25.50%	16.55%	8.94%
p2675	48,267	10.07%	24.89%	24.41%	0.48%
p4207	96,651	8.52%	19.47%	12.24%	7.24%
p4210	113,877	12.05%	22.60%	10.58%	12.01%
p5918	119,979	7.54%	16.09%	10.07%	6.02%
p6291	161,352	10.65%	14.75%	7.50%	7.25%
p7318	238,464	25.42%	4.89%	4.82%	0.07%
p7890	182,826	9.38%	10.26%	6.61%	3.65%
p9041	276,642	6.00%	16.57%	4.51%	12.06%
p10705	279,594	10.27%	11.36%	4.42%	6.93%
p12292	268,830	6.11%	20.08%	4.64%	15.43%
p13033	332,478	9.62%	11.59%	3.67%	7.92%
p13651	308,727	8.48%	4.18%	3.91%	0.27%
p14473	333,612	9.31%	34.15%	3.87%	30.27%
p17828	521,712	14.93%	6.75%	2.40%	4.34%
p22383	697,527	6.23%	20.90%	1.97%	18.93%
p23572	774,684	7.95%	10.34%	1.64%	8.70%
p24370	552,096	5.57%	19.61%	2.92%	16.69%
p25015	616,887	10.69%	5.93%	1.99%	3.95%
p27530	542,394	3.32%	15.36%	2.32%	13.04%
p44177	1,324,980	12.38%	4.42%	0.95%	3.47%
p52251	1,482,687	14.19%	1.50%	0.88%	0.61%
p52922	1,889,622	9.34%	8.42%	0.86%	7.57%
p64984	1,714,725	14.71%	11.26%	0.80%	10.45%
p80590	2,492,622	4.94%	2.91%	0.58%	2.33%

Table 3: Silicon area

The silicon area for the LFSR, MISR, and test controller can be considered as the lower bound on silicon area for pseudo-random BIST. Since we applied 10,000 pseudo-random patterns to all circuits, the size of the required LFSR, MISR, and test controller is almost constant for all circuits. Hence, as shown in Table 3, the percentage of silicon area decreases with increasing circuit size to less than 1% for the largest circuits. With increasing circuit size, the sequence-generating logic tends to be the major part of the BIST hardware.

For circuits larger than 5K gates, the total silicon area for BIST with 10,000 patterns is typically 5-15%. Of the 20 circuits larger than 5K gates, 5 circuits require less than 5% silicon area, 9 circuits require 5-15% silicon area, and the 6 remaining circuits require more than 15% silicon area. In addition, 3 of the 5 circuits larger than ~50K gates require less than 5% silicon. In several cases, e.g. for the 5 largest circuits with more than ~50K gates, the total area for deterministic BIST is less than the area for the scan design.

The size of the sequence-generating logic primarily depends on the random-testability of the circuit. Circuits that are badly random testable require a larger sequence-generating logic than circuits that are well random testable.

A trade-off is possible between test time and silicon area. When increasing the number of patterns, the test time increases but less silicon area for the BIST hardware is required. In all experiments so far, we applied 10,000 test patterns, which is relatively small. Increasing the number of pseudo-random test patterns provides higher random fault efficiency, and in addition the degree of freedom for embedding deterministic patterns is enhanced. Both effects cause that the silicon area for the sequence-generating logic decreases. These effects are clearly demonstrated in Table 4. In all cases reported in Table 4, the fault efficiency obtained with deterministic BIST is >99.9%.

circuit	#test patterns	FE$_{\text{rand}}$	BIST silicon area		
			total	LFSRs & test control	SGL
p9041	10,000	97.00%	16.57%	4.51%	12.06%
	32,768	97.54%	14.50%	4.67%	9.83%
	65,536	98.24%	13.83%	4.88%	8.95%
	131,072	98.24%	12.63%	4.98%	7.65%
	262,144	98.24%	11.85%	5.09%	6.75%
p14473	10,000	86.39%	34.15%	3.87%	30.27%
	65,536	91.01%	30.27%	4.20%	26.07%
	131,072	91.01%	28.16%	4.24%	23.92%
	262,144	91.01%	28.09%	4.32%	23.78%

Table 4: Trade-off between test time and silicon area

A trade-off is also possible between test quality and silicon area. It is generally known that the major part of an ATPG test pattern set is required for detecting the last few percents of undetected faults [BASS89, HETH99]. A similar observation can be made for deterministic logic BIST: most silicon area in the sequence-generating logic is required for detecting the last remaining undetected faults. This is clearly demonstrated in Table 5. Decreasing the target fault efficiency from 100% to 99% may result in reduction of half the silicon area for the sequence-generating logic.

circuit	FE$_{\text{BIST}}$	BIST silicon area		
		total	LFSRs & test control	SGL
p9041	100%	16.57 %	4.51 %	12.06 %
	99.00%	10.41 %	4.51 %	5.90 %
	98.00%	7.03 %	4.51 %	2.52 %
	97.00%	4.51 %	4.51 %	0 %
p14473	100%	34.15 %	3.87 %	30.27 %
	99.00%	25.09 %	3.80 %	21.29 %
	96.00%	16.21 %	3.75 %	12.46 %

Table 5: Trade-off between test quality and silicon area

5. Conclusions

We presented the application of a deterministic logic BIST scheme on industrial designs. Our experimental results show that complete fault coverage can be achieved for circuits up to 100K gates with 10,000 test patterns at a total area cost for BIST hardware of typically 5-15%. The size of the BIST hardware primarily depends on the random testability of the CUT.

We also demonstrated that a trade-off can be made between test time, test quality, and silicon area. For circuits that are reasonably well random testable, the size of the BIST hardware may be reduced to typically less than 10% by increasing the test time (i.e. the number of test patterns). Decreasing the target fault efficiency from 100% to 99% may result in a reduction of half of the silicon area for the sequence-generating logic.

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