IEEE 1149.4 Analog and Mixed-Signal Test Bus Standard

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ABSTRACT

The Analog and Mixed-Signal Boundary-Scan Standard (IEEE1149.4 hereafter referred as dot4) was developed to measure external discrete components in a mixed-signal Printed Circuit Assembly (PCA). This bus uses 4 of the same signals used today to support IEEE1149.1 compliant devices and systems. It uses two additional wires bus to perform analog monitoring and control.

But testing a mixed-signal PCA is a crucial issue not only when the PCA is a traditional board but also for what is often its natural evolution: System on Chip (SoC) with embedded mixed-signal module. Although the original intention of the boundary-scan standard was to make provision for mixed-signal chips on boards of all kinds, SoC testing solutions cover the needs for board testing.

This paper describes the basic architecture of the test bus, gives some system measurement methodologies and provides basic examples of usage.

1   INTRODUCTION

A consortium of IC vendors, IC users, Automatic Test Equipment (ATE) vendors, universities and R&D institutions developed the IEEE1149.4 Standard. This consortium formed a Working Group almost one decade ago and in March 1999 the standard was approved by the IEEE [1]. A minimum of three meetings per year was held with reported minutes [2].

In the eighties, boards and integrated circuits were mainly tested functionally. The principle of constructing electronic circuits in this way has been a standard practice for several decades. For much of this time, the testing of such PCAs has relied on the use of an in-circuit tester, which applies mechanical probes to the individual component pins. This allows each component to be tested effectively in isolation, by applying test signals to the component inputs and monitoring the test responses at the component outputs as shown in Figure 1.

But then, due to the need of efficiency in the test of digital boards, IEEE1149.1 emerged in 1990 [3][4].
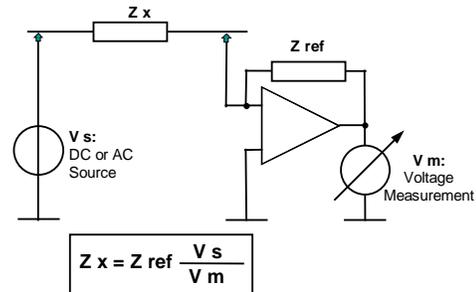

$$Z_x = Z_{ref} \frac{V_s}{V_m}$$

Figure 1 - Analog In-Circuit Test

Up to then, due to the lack of efficient solutions for mixed-signal boards, these have been tested using traditional techniques. Although each company has its own solution, a usual approach consists in mixing dot1 for the digital part of a board and traditional in-circuit test technique for the analog part (Figure 2).
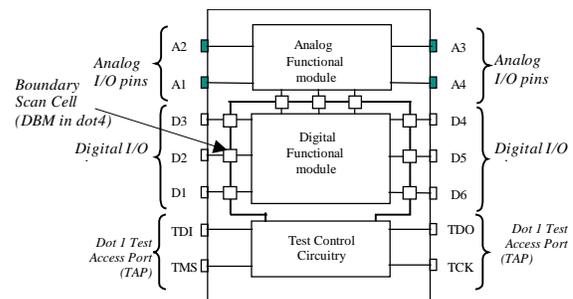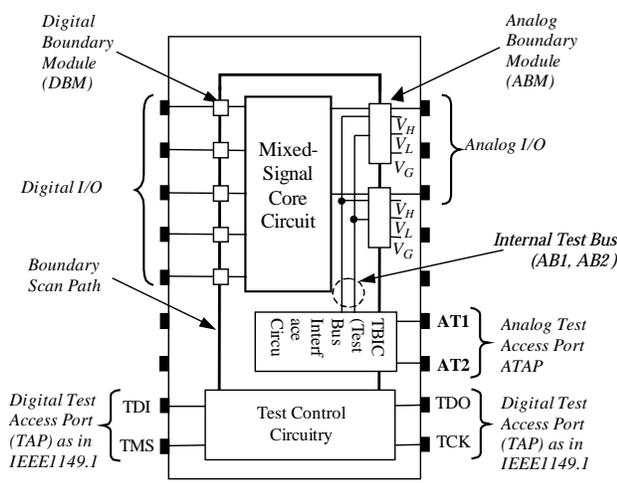

**Figure 2 -** Mixed-Signal Dot1 Chip

2   TEST BUS ARCHITECTURE

IEEE1149.4 defines an architecture that is to be designed into each mixed-signal device supporting the Standard. The architecture defines 6 pins on each device forming a bus. Four of the pins are the same as those defined for the IEEE 1149.1 Test Access Port (TAP) [4] and act in conformance to all the rules defined in that Standard. The 1149.1 bus carries the control information for setting up the test architecture in support of a measurement scenario. It can also be used to perform a traditional interconnect test as is usually done using the 1149.1 EXTEST instruction, but now to include the analog function pins of a device.

Figure 3 - Basic Mixed-Signal Dot4 Chip Structure

2.1 Boundary Modules (DBM and ABM)

In dot4, every pin is required to have a boundary module associated with it (Figure 3). In the case of the digital pins, the boundary modules (DBMs) are identical to the boundary-scan cells defined in dot1, except that there is an option to extend the facilities using a form of analog boundary module (ABM) if enhanced (analog) measurement capabilities are required [5].
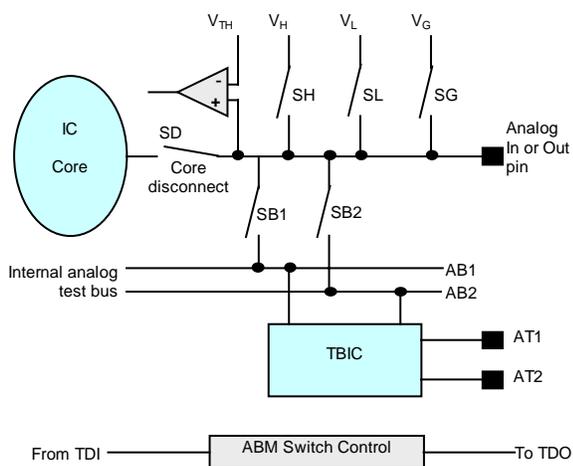
Figure 4 - Architecture of ABM

A standard ABM consists of a switching network connected between the pin and the core circuitry, allowing the pin to be put into a state, in which it is isolated from the core, and to be connected to a DC voltage or an internal analog test bus line: V_H, V_L or V_G.

2.2 Test Control

Each DBM contains a memory element that can store logic test stimuli or responses [6]. These memory elements appear as part of the boundary-scan register, and are accessed by external test equipment through TDI and TDO under the control of the TAP controller.

The ABMs are also controlled digitally, the operation of the switches in each ABM being determined by the contents of its individual control register. The control register can also be used to capture digital test results, representing either logic values or digitized analog responses. All the ABM control registers are included in the boundary-scan register, which can therefore be loaded and unloaded through the TAP as with the DBMs.

2.3 ATAP

To support the analog stimulus and response capabilities of dot4, two two-wire test buses are involved: a board-level bus carrying signals between the test equipment and the chip, and an internal one that distributes the signals round the interior of the chip (AB1 and AB2). Access to the internal bus is through a dedicated pair of pins that constitute the analog test access port (ATAP).

2.4 TBIC

The test bus interface circuit (TBIC), takes the form of another switching structure, allowing each of the internal test bus lines to be connected to either or both ATAP pins or to be isolated from both of them. Isolation of the internal test bus when not in use is necessary to avoid unwanted interference and cross coupling.
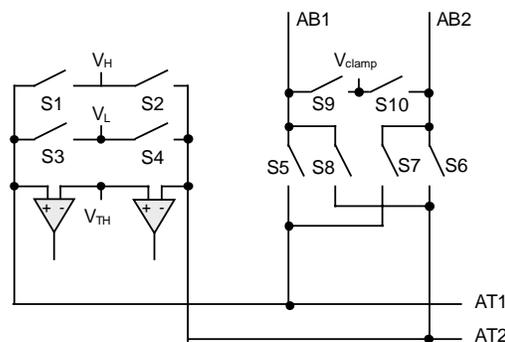
Figure 5 - TBIC Switching Architecture

3   INSTRUCTION SET

In this section the instructions that are used in 1149.4 are reviewed. These instructions are almost identical to those for an 1149.1 compliant IC. Only an instruction called PROBE must be added. However most of the 1149.1 instructions are interpreted differently for analog pins. Mandatory instructions are: BYPASS, SAMPLE/PRELOAD, EXTEST and PROBE. This last instruction is described below.

Optional instructions are: INTEST, CLAMP, HIGHZ, RUNBIST, IDCODE and USERCODE.

The table below [5] summarizes the IEEE 1149.4 instruction set:

Instruction	Requirement	Mode of function pins
BYPASS	Mandatory	Function
SAMPLE/ PRELOAD	Mandatory	Function
EXTEST	Mandatory	Test
PROBE	Mandatory	Function
INTEST	Optional	Test (digital pins) Function (analog & clock pins)
CLAMP	Optional	Test
HIGHZ	Optional	High-Z (digital pins) CD-state (analog pins)
RUNBIST	Optional	Test (output pins) Function (input pins)
IDCODE	Optional	Function
USERCODE	Optional	Function

Table 1 - IEEE 1149.4 Instructions summary

3.1   PROBE

This instruction is the only one related to IEEE 1149.4 exclusively. PROBE provides a real-time virtual scope probe capability to devices compliant with the P1149.4 Standard. Although obviously bandwidth limited, this feature allows the monitoring of signals at AT2 as they flow around a system while the system is performing its mission function. Similar in nature to 1149.1's SAMPLE instruction, it differs in that a continuous view of a signal in time is allowed. Designers looking at system and environmental interactions should appreciate this feature of the Standard. While the PROBE instruction is active, AT1 is also capable of injecting a signal into the device. One should note that this could be a dangerous facility, and should be used with caution [5].

4   MEASUREMENT PRINCIPLE

Traditional board testing is based on in-circuit test technique providing direct physical access to each pin of each chip on the board, through a dedicated test head fixture called "bed-of-nails". Defects to be detected here are of mechanical, thermal and electrical types. Full observability and controllability would be guaranteed with these methods if all the nodes on the board were accessible. However, this is unrealistic in case of several layers boards as well as Multi-Chip Modules (MCM) and double-sided boards with Surface Mounted Devices (SMD) on each side.

With the in-circuit technique, an interconnect testing is performed to measure external passive components and to diagnose for possible defects.

The failures to be detected on a mixed-signal board, either with the bed-of-nails technique or with any other method, can be classified in four categories (Figure 6):

- Shorts between two digital signals, two analog signals or between an analog and a digital signal
- Opens in direct connections or in the impedance links to the circuits
- Missing components like a mixed-signal or a digital circuit or one of the impedances Z1, Z2 and the pull-downs (or pull-ups)
- Wrong component type or value of the mixed-signal or digital circuit or of the impedances Z1, Z2 and the pull-downs (or pull-ups)

(a)

(b)
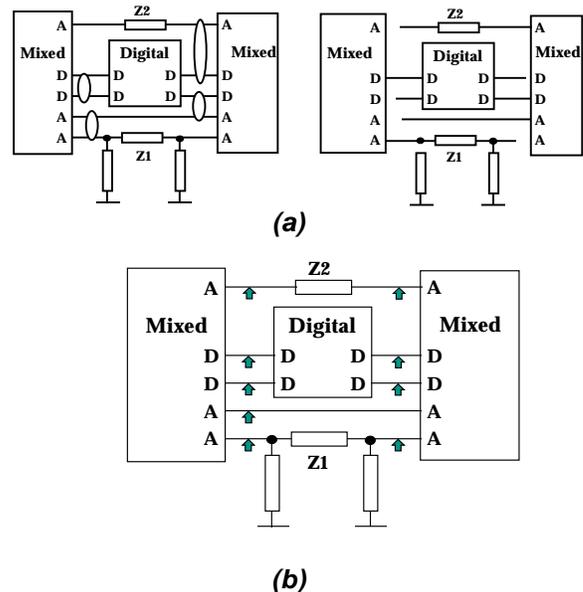
Figure 6 – *(a)* shorts & opens in mixed-signal boards & *(b)* Bed-of-nails board test method

The Z1 and Z2 impedances can be resistors, capacitors, inductors, diodes or circuits like filters, attenuators, etc.

In mixed-signal boards in general, passive components are often used between analog circuits to perform some specific functions, e.g., coupling or filtering [7]. Pull-ups and pull-downs are also often used in digital circuits for different purposes.

Figure 7 shows how an analog in-circuit testing would be performed. As for board in-circuit testing, the technique of dot4 measurement is based on the application of a current on one end of the external component and the measurement of the voltage appearing on the other end. Access to the Zx both ends is made through nails. Assuming that Zs and Zi are much smaller than Z1 and Z2, respectively, we can that since they are in parallel they can be neglected and Zx could then be calculated out of the measurement.

With dot4 the nails are replaced by access through switches using the structure of the ABM and TBIC. The metrology is finally identical and the final calculation of the impedance value is also identical.
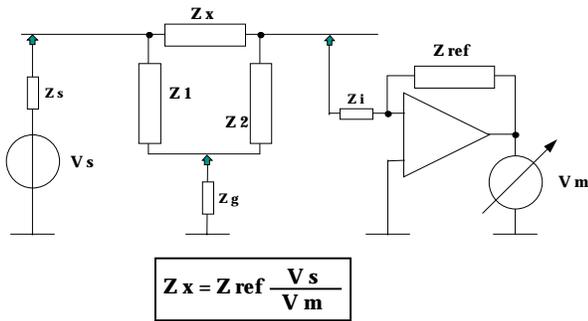

$$Z_x = Z_{ref} \frac{V_s}{V_m}$$

Figure 7 - Analog in-circuit test with guarding

Figure 8 shows an example where a resistor R1 is measured through the two pads of the same dot4 ship on which it is soldered. This two-wire measurement could be compared to Figure 1 where a current is applied through S5 and SB1 and the voltage is measured through S6 and SB2. The full path of the current application would be: Current source-AT1-S5-AB1-SB1-F1. And the voltage would be sensed through: F2-SB2-AB2-S6-AT2 then to the voltmeter on AT2.

But before testing the component itself against its ideal value, an integrity verification of the infrastructure is first performed. This verification checks the various analog-switching functions and the digital registers. Once this verification is done the test of the chip can start [8].
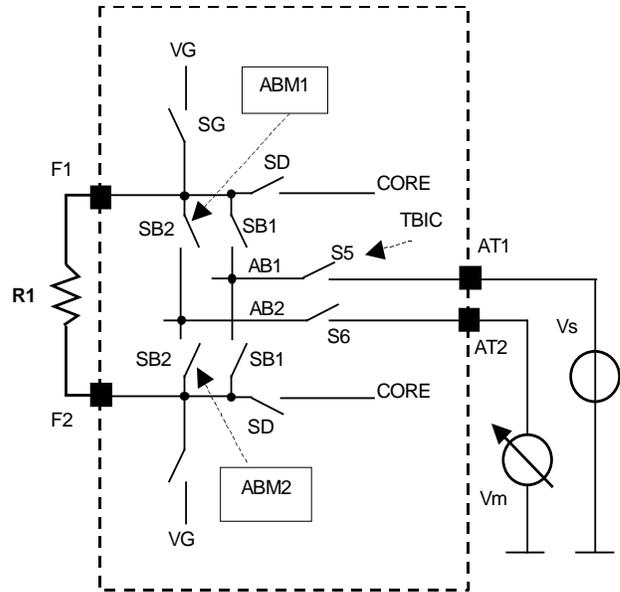

Figure 8 - Dot4 Two Terminal Measurement

5   CONCLUSION

1149.4 was developed as a standard to measure external discrete components in a mixed-signal Printed Circuit Assembly (PCA). This standard provides a structure for interconnect test, parametric test and other functional characterization of mixed-signal systems.

We can define the IEEE 1149.4 Analog and Mixed-signal test bus standard as built on the foundation of IEEE1149.1 with the ability of performing continuous time and continuous voltage/current access.

The standard is controlled by a set of instructions based on the 1149.1 instruction set plus one additional specific instruction.

IEEE 1149.4 can help improve system testability, time to market and even performance through the the miniaturization of interconnects and improved characterization. The main additional cost are some switches and their associated parasitics. Although this can be performed without compromising performance.

Although IEEE 1149.4 is intended for production testing it can also be used to access pin signals for debugging.

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