Static and Dynamic On-Chip Test Response Evaluation using a Two-Mode Comparator

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Abstract

A Design-for-Testability implementation to achieve high fault coverages in the analogue functional blocks of mixed circuit ASICs is presented in this feasibility study. To this end existing OpAmps or OTAs are converted into clocked comparators with hysteresis and variable reference levels. The resulting two-mode comparators are connected to specific internal nodes. Depending on the mode this node can be either statically and/or dynamically evaluated on-chip without the need to bring an analogue signal off-chip. Results from first simulations and measurements on a test circuit realised in 0.35 µm technology are presented.

I. INTRODUCTION

Many defects impacting integrated analogue circuits either affect the dc operating point of the circuit or its dynamic behaviour. Therefore it is not sufficient to only test for dc levels. On the other hand dc tests are fast and cheap, whereas dynamic tests are time consuming. However, if complex mixed-signal ASICs have to be tested, the accessibility to respective nodes that have to be observed is not always given. Moreover, unlike during prototyping, in production a type of GO/NOGO test is also performed for circuit specifications, whenever possible. One possible solution to support the GO/NOGO test is the implementation of simple comparators as long as they do not require too much effort. Comparators have already been proposed before, however, for different purposes. One example is an extension to the IEEE boundary scan standard 1149.4 for mixed signal ICs [1]. It is referred to as “Analogue Early Capture” and comprises of a strobed comparator with a variable threshold to be used as a waveform digitiser. Of course the design requirements for such a digitiser, however, are high in terms of meeting the Nyquist bandwidth as well as the clock skew and jitter. Another interesting application is to use a comparator to measure the performance of sense amplifiers in SRAM’s [2]. For this purpose a dedicated differential comparator is integrated into a SRAM. The dynamic performance is measured by comparing the differential sense amplifier signal of the SRAM’s with an externally applied differential signal. Very recently a digital comparator has been proposed as a low cost alternative for the observation of internal circuit nodes of mixed-signal ICs [3].

However, for a fast GO/NOGO testing of analogue circuit nodes at different signal levels an analogue comparator is required. Such comparators can be realised with only few additional transistors by converting existing OTAs or operational amplifiers (OpAmp). The advantage of this approach is the same as for the functional conversion of system registers for digital Built-In Self-Test. The amount of extra test specific circuitry is limited and, thus, defects affect both the test circuitry and the circuit under test.

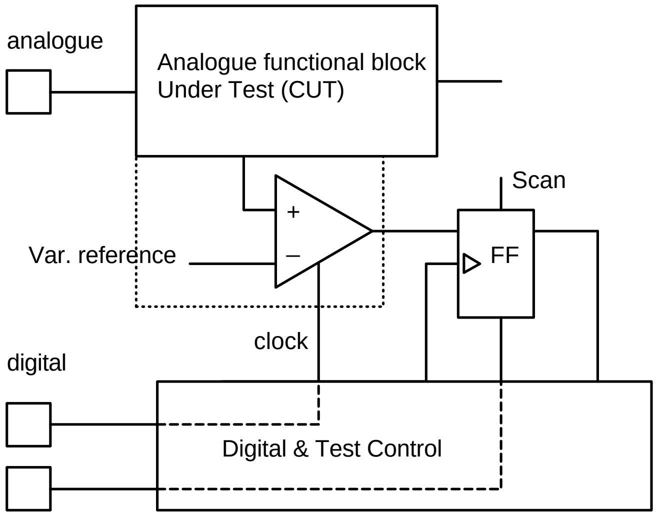

Fig. 1 Basic scheme for the comparator based DfT scheme

The basic concept which can be adopted to the specific circuit situation is shown in Fig. 1. The circuit under test (CUT) is a functional block which is connected to a primary input (analogue pad). An appropriate node (test node), in general the output, of the CUT is connected to the comparator. The other comparator input is connected to a variable reference to allow the comparison of different dc levels and thus a binary decision (GO/NOGO). The variable references can be easily derived from the biasing circuit of an ASIC [4]. The output of the comparator is stored into a latch or flip-flop (FF) which in turn can be part of a scan path if implemented or directly connected to a digital output during test mode. Normally this latch or FF runs with the system or scan clock of the digital part. Thus, modifying the clock scheme of the FF for clocking the test node at different variable instances of time is in general not possible. Therefore a clock controlled two-mode comparator is proposed. It can be operated as a “clocked comparator”, or as a static comparator. In the latter mode the dc operating point levels can be checked under different static operating conditions, whereas the first mode is used to perform consecutive comparisons at different time instances within a certain time window. With this implementation it is possible to perform different fast tests under static and dynamic conditions of the CUT. Neither an analogue signal has to be brought off-chip nor an analogue signal for comparison has to be applied nor the exact specified parameter has to be measured. If the FF is part of a scan path the test result can be easily shifted out as a sequence of two or three binary digits which in turn can then be easily evaluated by an automatic test equipment without interfering the overall clocking scheme of the circuit. If the FF is not part of a scan path it can be used for the clocking and the comparator becomes even more simple.

II. TWO-MODE COMPARATOR AND TEST SCHEME

In the following the clocked comparator and the test scheme for which it is used are described, assuming that the FF is part of a scan path, which becomes more and more true also in cost critical ASICs.

Since the two-mode comparator is always clocked, though differently, the output becomes stable only after the settling time.

To avoid invalid data the FF is therefore used as a time filter with a maximum filter time of $1/f_{scan}$. This is the boundary condition for the design of the comparator and the clock for the comparator. However, there is also another design condition for the implementation of the comparator that has to be included.

Whether or not a comparator switches at the correct level depends at first on the g_m of the input stage, which can be controlled by the W/L and the biasing current, but also on the slew rate of the output stage. Besides this it is the overdrive that is necessary to toggle the comparator which determines the switching delay. A slow input signal causes a high delay, since it needs more time until the necessary overdrive is reached, whilst a steep input signal rapidly toggles the comparator. This has to be taken into account for the design since otherwise a wrong signal is latched. Another aspect for the design is related to the fact that basically dc levels are compared in static test mode and also for the last comparison in the dynamic test mode.

Assume that the actual dc level to be compared is close to the reference level, then the comparator will start to switch randomly due to noise or temperature drifts (Vth drift) and a non-valid response is latched. To avoid this oscillating effect, the comparator must be designed with a hysteresis. The hysteresis and the test procedure using the hysteresis are depicted in Fig. 2.

The test procedure for which the comparator is used comprises for each evaluation of a two step binary search with two reference levels, i.e. ref. 1 and ref. 2, used to detect whether or not the actual dc value falls into or outside the tolerance band of a good CUT. In Fig.2, this tolerance band is indicated by the shaded area. The knowledge of this area is necessary for the adjustment of the two reference levels ref. 1 and ref. 2. The tolerance band can be obtained in various ways e.g. from a worst-case simulation, a Monte-Carlo analysis or from previously measured characterisation data. The dotted lines (1 –5) indicate different possible dc levels for the comparison and the two bold lines show the two reference levels ref. 1 and ref. 2.

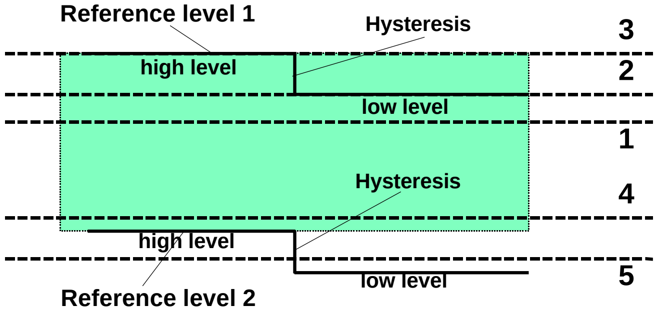

Fig. 2 Hysteresis and reference levels for different dc inputs (1-5)

The test procedure for each comparison is simple and as follows: the reference levels are adjusted such, that the high level coincide with the upper limit (ref.1) and the low level with the limit (ref.2) of the tolerance band, respectively. Since the actual signal level is not known, noise and temperature drifts can not be excluded the comparator thresholds are lowered to the low level once the comparator has switched. By this, bouncing and ringing on the comparator output can be prevented. Of course the hysteresis has to be such that it is large enough to ensure a secure detection. As can be seen from Fig. 2 for all depicted signal level (1-5) a secure detection without ringing effects is possible, also in particular for the signal level 2. Up to now dc levels were assumed. However, it is also intended to use the comparator for the evaluation of dynamic signals and, thus, the overdrive is an important parameter as it contributes to the inherent delay of the comparator itself. In the proposed DfT implementation, however, the time for the comparison can be controlled by the comparator clock and thus, chosen such, that enough overdrive is present to ensure a fast switching.

The comparator can be obtained, by exploiting system OTAs (M1-M5) and OpAmps, respectively. The principle functional conversion is illustrated in Fig. 3. To this end during test mode first the differential system input pair (M1, M2) is powered down by M6. The active load (shared with the system input pair) is connected to the differential input pair (M7, M8) of the comparator. The comparator pair is designed for high speed, i.e. appropriately biased by the current source M10. Furthermore, the OTA is buffered to avoid slew rate problems (not depicted here). Consequently, the two mode-comparator can be implemented at relatively low overhead and also shares the load transistors M3 and M4.

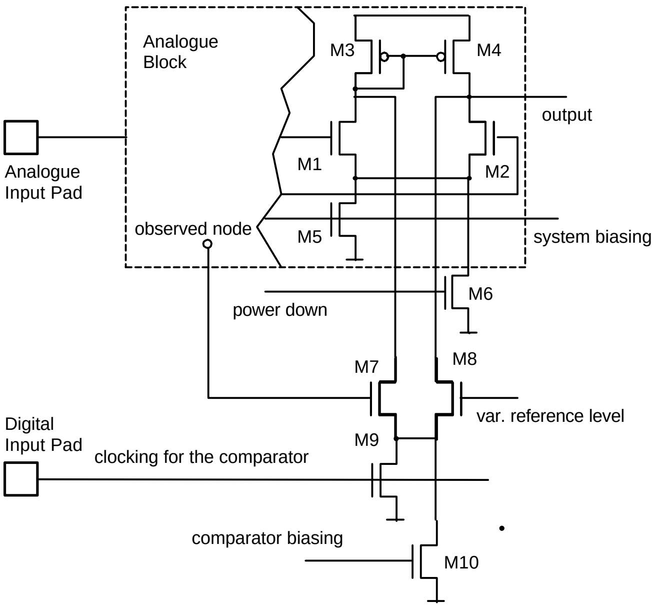

Fig. 3 Principal hardware convertion for the comparator

During test mode the comparator can be clocked (M9) via an multiplexed digital input. The two reference levels are derived from the central biasing stage and applied to M8 as described in [4]. Since the system biasing line in general is also connected to further current sources of the circuit supplied by the same current mirror, M5 can not be powered down by pulling the gate of the current source M5 to ground. If this applies, an additional power-down transistor M6 is needed. This transistor can also be used to power down the OTA during Iddq test if the circuit was supplied from the digital supply for some reason. To avoid that an analogue input must be used to bias and clock the comparator, an extra transistor for the clocking of the comparator is added (M9). This allows to use a digital input for the comparator clocking whilst the comparator biasing can be done on-chip. Moreover, the clocking can be easily controlled by an automated test equipment. In general dummy switches have to be used to compensate for charge injection during the clocking rather than a single transistor as shown here. However, it seems that this could be avoided due to the filter time property of the FF on the output of the comparator and the control over the comparator clock.

III. Simulation and Measurement Results

A general purpose 0.35um technology test circuit (Fig. 4) designed for different investigations was used as case study, in this work. Since it was also used for investigations dealing with radiation hardness the NMOS transistors were layouted as edgeless or closed geometry transistors [4] as shown in fig. 5. By changing the bias of the transistors it is possible to configure it in different ways (cascode, OTA, folded cascode). In this work the circuit was configured as a cascode. In the cascode configuration (fig. 4) M2, M3 and M4 are powered down, whereas M0 and M1 form the active load of the cascode constituted by M5 (common gate) and M6 (common source). Note, that the circuit was not optimised for the above purpose.

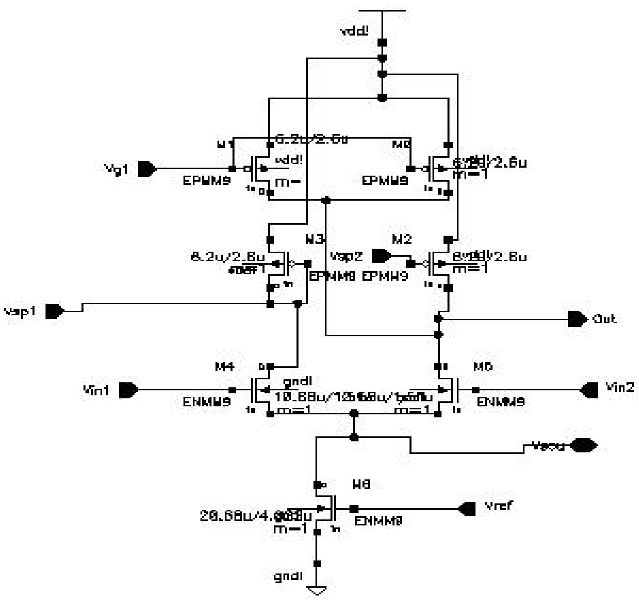

Fig. 4. Schematic of the configured test circuit as circuit under test (M0, M1, M5, M6)

The layout of the test structure (Fig. 3) shows on the top the four PMOS transistors (M1, M0 in Fig.4), whilst the two small and the one large closed geometry NMOS transistors are placed below.

In our investigations the simple cascode was connected to an OTA also available on the test chip used as a clocked comparator. The hysteresis was realised by using a positive feed-back where the reference voltage was connected to via a voltage divider.

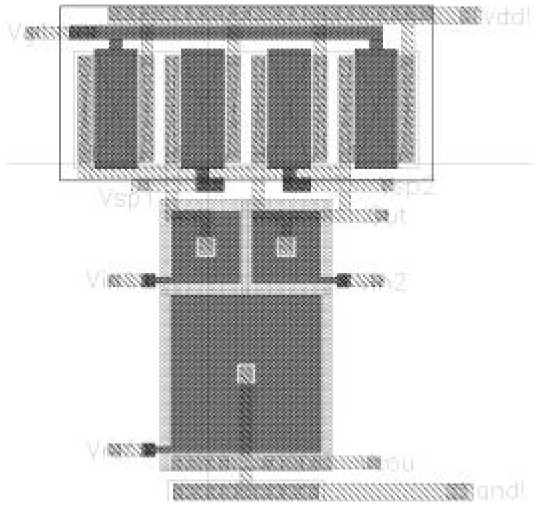

Fig. 5 Layout of the circuit under test shown in Fig. 4.

Unlike in the real functional conversion of an OTA or OpAmp, the test chip comparator was clocked and biased via the same transistor. Also the reference levels of the comparator were applied externally.

As dynamic test stimulus the so-called COMPSIG stimulus [5], [6], [7] was applied. As known from there, the response of a good circuit to the COMPSIG vanishes for t= (n+1)T, with T chosen such that the test signal spectrum covers the nominal network bandwidth.

As a result, the test signal design is sensitive to pole perturbations. In this case a zero input response signal on the observed output has to be detected. In case of a good circuit, the comparator does not switch for reference level 1 but for reference level 2 when the response is checked after (n+ 1)T. However, this could also be due to a fault inside the comparator.

To avoid this the first comparison is done while the response of the CUT is still changing (dynamical evaluation), i.e. during transient of the response. The time for the comparison is chosen such, that for a good CUT the comparator switches. This means, that the first evaluation of the test response is started before the output signal settles to the steady-state after t=(n+1)T.

In the following results from simulations and measurements are presented and discussed.

As mentioned the cascode was stimulated with its COMPSIG stimulus. The higher threshold level of the comparator was set to the value of the normal output offset of the cascode (steady-state for zero input) plus a margin of 400mV. The tolerance band was previously found from worst-case simulations.

Fig. 6 shows the results of the simulation for the good circuit with typical parameter values at ambient temperature.

Due to the chosen biasing, the zero-input response of the cascode output is at 2.48V. This is also the dc level to which the output of the cascode returns after (n+1)T.

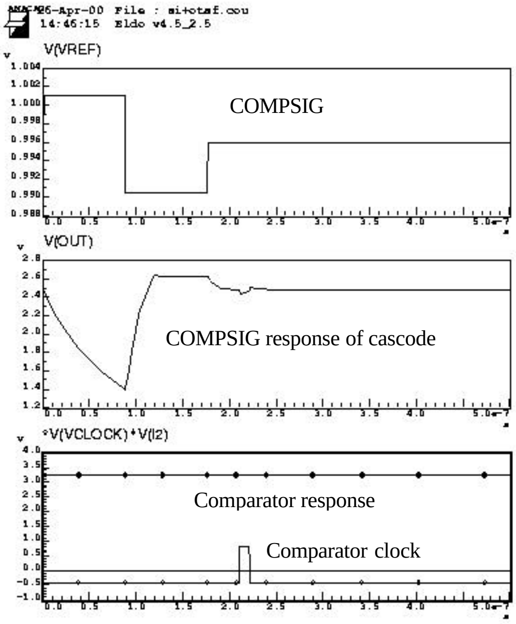

Fig. 6 COMPSIG test stimulus used for the cascode CUT and response of the fault free circuit.

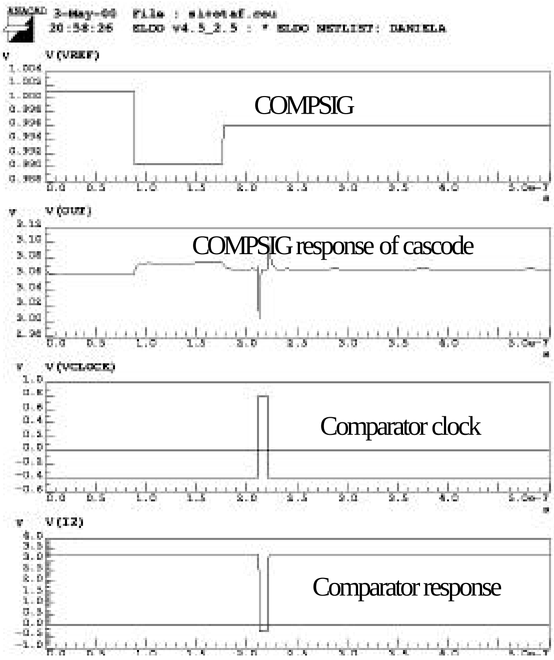

Fig. 7 Simulations results in presence of a short between the gates of the transistor M5 (Vref) and M6 (Vin2)

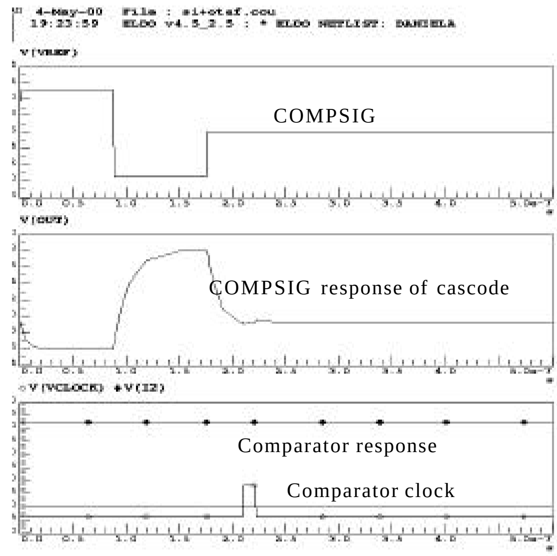

Fig. 8 Simulation results for a parametric fault.

As can be seen, the comparator did not switch (constant output signal) when the comparator was enabled by the clock, since the dc level at this moment (2.48V) is lower than the chosen reference level 1. Note, that the charge injection effect on the cascode output signal due to the switching is visible as a small over- and undershoot, respectively.

For the fault assumption the L^2RFM scheme [8] was applied. Due to the layout a spot defect could result in a short between the closed geometry NMOS transistor gates of the two cascode transistors M6 and M5 (cf.Fig. 4, Vref, Vin2). The result of this fault simulation is depicted in Fig. 7. Since now the COMPSIG response (cascode output) is higher than the applied threshold level, the comparator switches down when the comparator is enabled (clocked). Note, that due to the width of the clock pulse the comparator does not completely switch to zero. However, for a latch this is also not necessary, as long as it is lower than the digital threshold of the logic gate. If this is valid the latch captures the correct state of the test response as intended.The previous example showed a fault that rendered the CUT into a catastrophic failure mode, where no COMPSIG response could be observed.

Therefore, in the next example (Fig. 8) a fault was injected that rendered the CUT into a parametric failure mode. Here a “mismatch” in the threshold voltage (Vth) between the two active PMOS loads (M0, M1) of the cascode was simulated. In this case the dc output level of the cascode decreases to 440mV, thus, below the comparator threshold level. Note that the cascode still reacts to the COMPSIG stimulus. Consequently the clocked comparator doesn’t switch. If however, the reference level is lowered to a value below 400mV (reference level 2) it evidently will switch as shown in the next figure (Fig. 9). The simulation result in Fig. 10 has been compared with bench measurement shown in Fig. 12.

In this configuration the transistor M0 and M1 are switched off and the transistor M2 is enabled. Because all these transistors have the same aspect ratio, it results in a reduced bias current inside the cascode. This simulates a fault on the biasing part of a circuit. The measurement under this abnormal behaviour of the circuit is compared with the normal one. Fig. 11 depicts the COMPSIG stimulus, the response of the cascode stage and the comparator when no fault condition is applied. During this measurement the comparator was left always on and a square wave between the high and the low reference level of the comparator was applied to the non inverting input of the OTA (Fig.11). Since the test circuit is a CMOS circuit it has to be protected by ESD clamps on the gate and also on the output to protect the drain junctions.

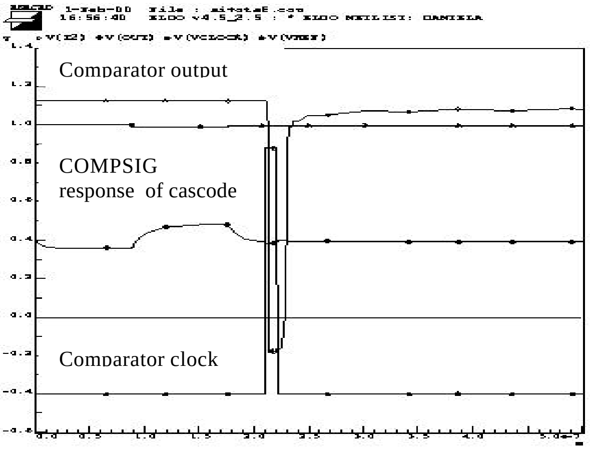

Fig. 9 Same situation as in previous faulty condition (Fig. 8) but at threshold level 2

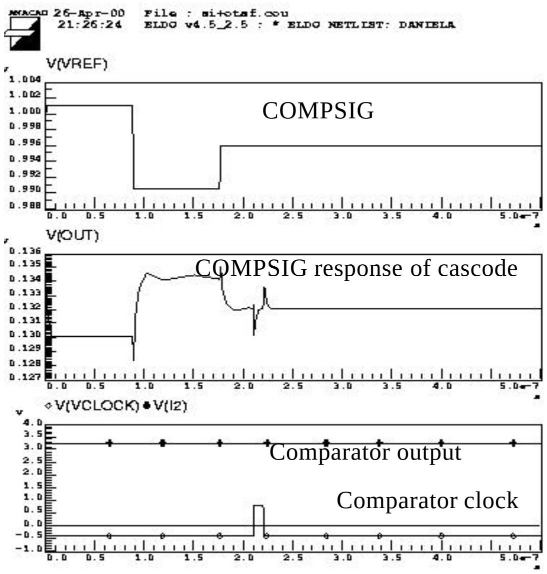

Fig. 10 Faulty condition reproduced during the measurement

To protect the gate on the input those clamps basically comprise of a large diode to the supply and a clamping circuit to ground and a resistor between the pad and the internal input node. On the output to protect the drain-bulk junction against break-down only a diode to the supply and a claming circuit to ground is implemented. However, for the COMPSIG signal design the impact of the ESD protection circuits has to be included and thus, the frequency of the test stimulus is lowered. Taking this into account, the simulation and measurement match. Note, the different scales for the COMPSIG (5mV/div) and the test response (100mV/div). The test response of the above fault condition were evaluated by the comparator with a reference level 1 higher than the typical zero response level of the cascode (2.48V) e.g. 2.56V and then to a reference level 2 of e.g. 2.4V. For the fault-free test response the comparator does not switch for the first comparison, but for reference level 2 as intended. Consequently the bit stream is "01". In case of the biasing failure the comparator does not switch at all, since for both reference levels the dc level of the cascode is below the reference levels 1 and 2 (Fig. 12). As a result the bit stream is "11". Note that this applies to a comparator with the reference connected to the non-inverting input.

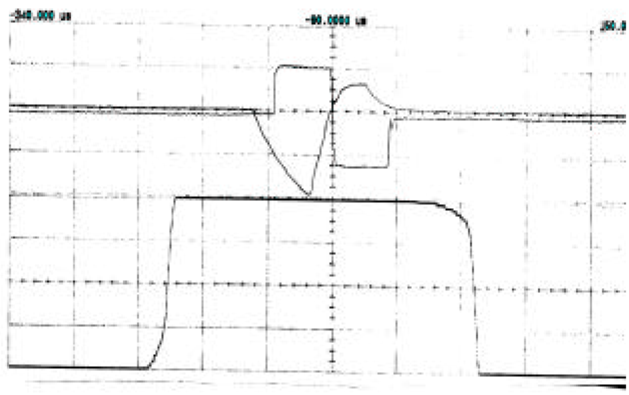

Fig. 11 Test stimulus: 5mV/div, time scale 20µs/div; measured test response cascode: 100mV/div, time scale 20µs/div; comparator output: 400mV/div, offset 2.4 V, time scale 50µs/div.

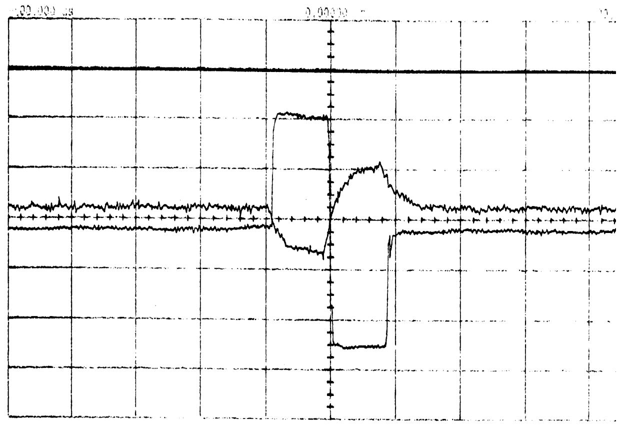

Fig. 12 Comparator output: 500mV/div, offset 1.75V, time scale 20µs/div; test stimulus: 2mV/div, time scale 20µs/div; measured cascode response: 5mV/div, time scale 20µs/div.

IV. CONCLUSION

A simple Design-for-Testability scheme has been described that is uses a functional conversion of existing OTAs or OpAmps. Those components can be easily converted into two-mode clocked comparators with hysteresis. This allows for a simple GO/NOGO test under production conditions. Neither an analogue signals has to be brought off-chip nor an analogue signal has to be fed. The implementation can be accommodated in scan path and potentially in the 1149.4 boundary scan scheme. Simulation and measurement results demonstrated the feasibility.

REFERENCES

[1] K. Leifstrom: "Early Capture for Boundary Scan Timing Measurements", ITC, paper 15.3, pp. 417-422, 1996.
[2] R. D. Adams, E. S. Cooley, P. R. Hansen, "A Self-Test Circuit for Evaluating Memory Sense-Amplifier Signals", ITC, pp. 217-225,1997
[3] D. De Venuto, M. Ohletz, B. Riccò, "On-Chip Checking of Analogue Circuits" submitted for publication in IEE April 2000
[4] D. De Venuto, M. J. Ohletz, "Bias-Programmable Hardware Reconfiguration for On-Chip Test Response Evaluation", accepted for publication IMSTW, Motpellier, June 23-26, 2000.
[5] H.H. Schreiber: " Fault Dictionary based upon Stimulus Design", Trans. Circuits and Systems, Vol. 26, No. 7, July 1979.
[6] F. Corsi, D. De Venuto, C. Marzocca: "A time domain technique for analogue filter testing", Proc. of IEEE ETW, Cagliari, May 28-30, 1997.
[7] D. De Venuto, F. Corsi, M.J. Ohletz: "Testing the analogue front-end of a mixed-signal pixel detector circuit using the complementary signal", Proc. of 4th IEEE Inter. Mixed-Signal Testing Workshop, June 8-11, 1998.
[8] M. J. Ohletz, " Realistic Faults Mapping Scheme for the Fault Simulation of Integrated Analogue CMOS Circuits", proc. ITC, pp.776-785, 1996