Current Testing Procedure for Deep Submicron Devices

Anton Chichkov
anton.chichkov@mie.alcatel.be

Dirk Merlier
dirk.merlier@mie.alcatel.be

Peter Cox
peter.cox@mie.alcatel.be

Alcatel Microelectronics
Westerring 15
9700 Oudenaarde
Belgium

Abstract

This paper presents a test technique that employs two different supply voltages for the same Iddq pattern. The results of the two measurements are subtracted in order to eliminate the inherent subthreshold leakage. Summary of the experiment carried out on "System on a Chip" (SOC) device build in 0.35m technology is also shown. These experiments proved that the method is effective in detecting failures not detectable with the single limit Iddq.

1. Introduction

Testing of digital integrated circuits generally involves use of a number of different test techniques as part of a test suite. Techniques as SCAN, BIST, V-stress, and Iddq are widely used in the industry [1].

The merits of Iddq testing in quality improvement, test cost reduction and burn-in elimination have been well recognized [1][2][3]. However, the effectiveness of conventional Iddq testing in deep sub-micron is eroded owing to the increased sub-threshold current in MOS transistors. The increasing leakage current levels are making the determination of the threshold that separates good from faulty ICs more and more difficult [4]. Many solutions have been proposed to contain the increased sub-threshold leakage [5]. These solutions include utilization of reverse biasing techniques to reduce the sub-threshold leakage in test mode, utilization of silicon on insulator technology for a sharper sub-threshold swing, or utilization of multi-threshold transistors to contain the sub-threshold leakage. Typically these solutions require non-trivial changes in the standard cell Library or in the process [6].

To overcome this limitation extensive work on statistical and ΔIddq methods has been done in recent years.

2. Prior Work

The idea of differential Iddq measurement have been around since it became clear that for deep sub-micron technologies the standard single limit testing is not anymore applicable. Several directions have been explored such as Δ over stress, Δ over patterns, dynamic current monitoring e.t.a. …

The technique Δ over stress includes measurement before and after stress test. In this case an evaluation of the current shift during stress is made. This technique combines the capability of voltage stress to highlight defects with the test coverage of Iddq.

In the technique of delta over patterns, the target method is based on the concept of differential current probabilistic signatures and on maximum likelihood estimation. The differential current measurement is defined as a difference between the Iddq taken at given vector and the Iddq at the previous vector. The use of differential instead of absolute current measurements is one of the features that distinguishes the method [7][8]. This use is highly motivated by the increasing importance of leakage current in sub-micron CMOS technologies [9].

The transient current testing (Iddt) has been often cited as an alternative and/or supplement to Iddq testing. Advantage of this method is that it is capable of catching device failures in the presence of raised background current levels. Furthermore the Iddt test can be carried out at a significantly higher speed than the Iddq [6]. However additional hardware and software will be required compared to an Iddq monitor.

3. Use of differential Iddq testing

Most of the previous methods are considering Δ over different test vectors. In this paper, an experiment is described taking Δ over supply voltage.

$$DIddq = Iddq(v_1) - Iddq(v_2)$$

The defects are highlighted by observing a too big shift in the current for a fixed shift of the voltage.

In order to prove the concept on experiment with a component developed in 0.35 μ has been carried out. To confirm that the result is relevant for the complete process window, a split lot was used. About 10000 devices from all corners of the process have been included in the experiment. The material has been tested with the standard Iddq method and with ΔV. On the Figure 1 can be seen the cumulative probability distribution of the different splits. This distribution is generated by a standard production analysis tool. What is shown on the figure is not the output of the tool. It has been reproduced for simplicity. Not all splits have been shown only the most relevant one’s. Also one strangely behaving split can be observed, the one drawn with circles.

For additional evaluation two samples have been taken from every split, one from the tail (marked with letter and number 2) and one from the main distribution (marked with letter and number 1). Exception from this rule is the split A because of its strange behavior four samples from different parts have been taken.

4. Results

The results form the measurements are shown in *Table 1*.

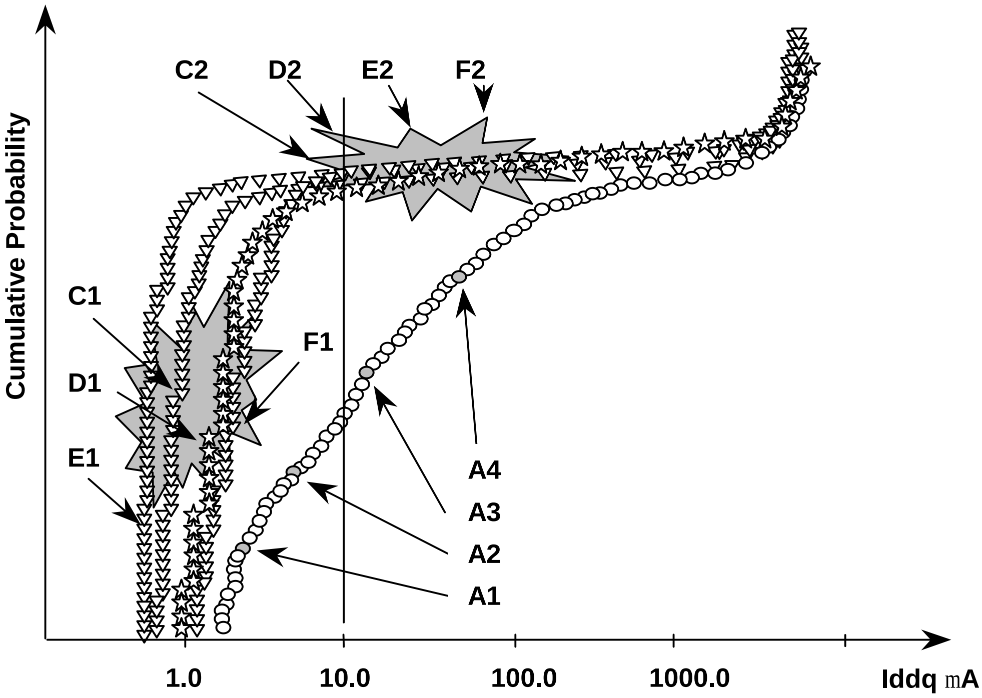

Figure 1 - Cumulative probability distribution of the different splits in a lot produced in 0.35μ technology

Split	Device N	Iddq at	
		2V	3.8V
A	1	3.90E-07	1.19E-05
	2	7.07E-07	4.56E-05
	3	1.43E-06	6.82E-05
	4	3.44E-06	2.63E-04
C	1	1.00E-09	1.09E-06
	2	1.00E-09	1.22E-06
D	1	4.80E-08	1.54E-06
	2	7.43E-07	1.17E-05
E	1	1.20E-08	9.76E-07
	2	4.26E-07	1.22E-05
F	1	8.50E-08	1.83E-06
	2	4.88E-06	9.31E-06

Table 1

On the fig2 the shift in current provoked by the shift in voltage can be seen. The split A has definitely a problem as the shift is too big and masks the rest of the results. To make rest of the results visible the devices 2, 3, and 4 from split A have been removed in *figure 3*. There is correlation between the place of the sample and the delta in current in *figure 3*. The only miscorrelation is sample 2 from split C after check was confirmed that the sample has been taken too close to the main distribution.

On *figure 4* the shape of the delta between this two measurements can be seen. It is clear that pass fail limit for delta measurement can be put at 1µA.

One of the most difficult tasks in Iddq testing is the definition of the pass fail limit. Interesting case is F split F2 device has relatively small increase because its first measurement is already high. F is the worst split for leakage, so high initial value is the expected result. It does not reflect defects, but it indicates that those devices are fast.

The decision to put the delta limit below or above 3µA will include this device in the good sample or not. Further investigation is ongoing on this subject.

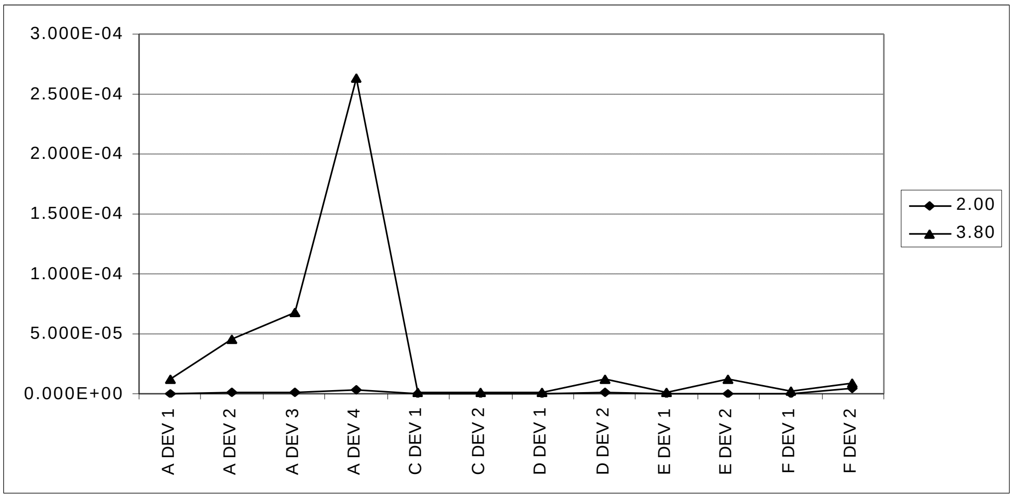

Figure 2 – Measurement on two power supplies for all splits.

5. Conclusions

In this paper a test technique that employs two different supply voltages for the same Iddq pattern has been described. The results of the two measurements are subtracted in order to eliminate the inherent subthreshold leakage. The summary of the experiment carried out on

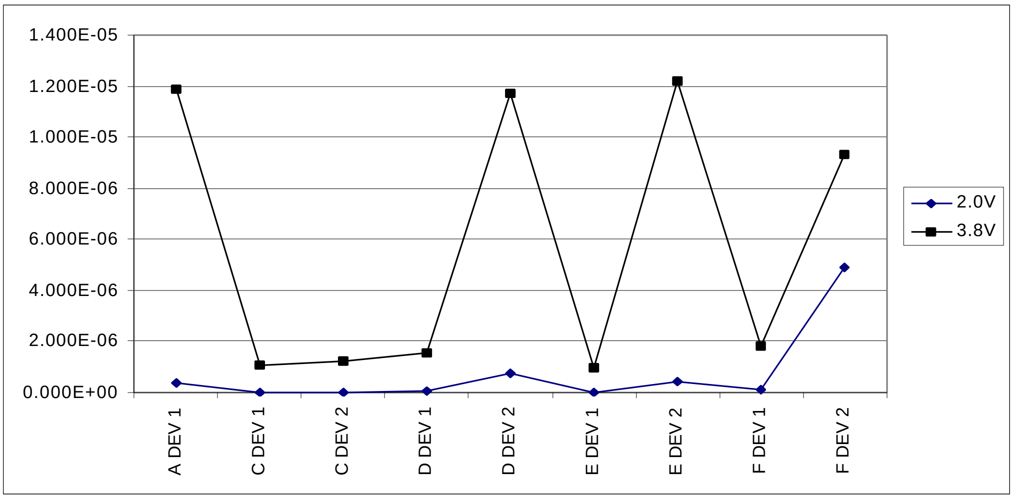

Figure 3 – Iddq measurements without split A(2,3, and 4)

complex device built in 0.35µ technology was shown. This experiment proved that the method is effective in detecting failures not detectable with the single limit Iddq. Special care was taken to ensure the statistical

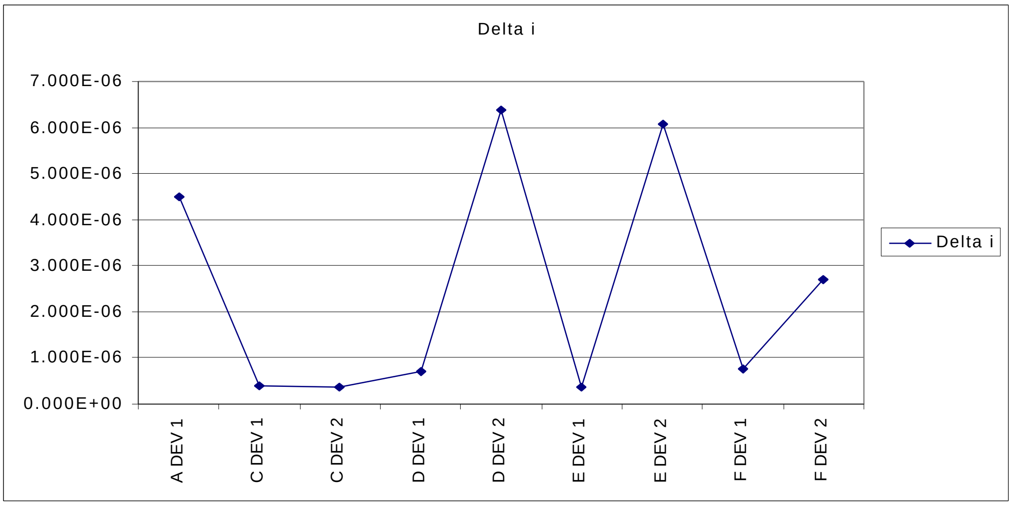

Figure 4 – ∆V Iddq

correctness of the results. A split lot was used for the experiment providing data from all corners of the process window. In every split more than 1500 devices have been tested to build the Cumulative Probability Distributions. Samples carefully chosen from relevant parts of the distribution made the evaluation of the method as complete as possible. This method has also the advantage of having less sensitivity to intrinsic leakage typical for deep submicron technologies.

6. References

1 P. Night, D. Vallett, A. Patel, and J. Wright, "Failure Analysis on Timing and Iddq-only Failures from the SEMATECH Test Methods Experiment" Proceedings of ITC98, pp43-52, October 18-23 1998 Washington, D.C. USA

2 A. Gattiker, and W. Maly, "Toward Understanding Iddq-only Fails" Proceedings of ITC98, pp174-183, October 18-23 1998 Washington, D.C. USA

3 Y. Okuda, I. Kubota, and M. Watanabe, "Defect Level Prediction for Iddq Testing" Proceedings of ITC98, pp900-909, October 18-23 1998 Washington, D.C. USA

4 A. Ferre, and J. Figueiras, " On estimating bounds of the quescent current for Iddq testing", Proceedings of IEEE VLSI Test Symp., pp 106-111, May 1996.

5 M. Sachdev, "Deep Sub-micron Iddq Testing: Issues and Solutions", Proceedings of ITC, pp786-792, 1996.

6 B. Kruseman, P. Janssen, and V. Zieren "Transient Current Testing of 0.25μ CMOS Devices", Proceedings of ITC99, pp47-56, September 1999 Atlantic City USA.

7 C. Thibeault. "An Histogram Based Procedure for Current Testing of Active Defects", Proceedings of ITC99, pp714-723, September 1999 Atlantic City USA.

8 C. Thibeault, and L. Boisvert. "Diagnosis Method Based on ΔIddq Probabilistic Signatures: Experimental Results", Proceedings of ITC98, pp714-723, October 18-23 1998 Washington, D.C. USA

9 J.M. Soden, C.F.Hawkins, and A.C. Miller, "Identifying defects in deep-submicron CMOS Ics", IEEE Spectrum, vol. 33 no.9, September 1996, pp 66-71.