A Fast I_{DDX} Monitoring Scheme for Testing Battery-Operated VLSI Circuits

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Abstract

Design and realization of an on-chip scheme for testing of deep-submicron low-voltage circuits using supply current-I_{DDX} monitoring is presented. The monitor is capable of detecting certain physical failures at significantly higher speeds than current sensors reported so far in the literature. The undesired effect of this scheme on the circuit-under-test performance is negligible for the voltage drop across the monitor is considerably minimized.

1. Introduction

Due to the advances in recent VLSI fabrication and market requirements, design trends have led to deep-submicron device geometries and consequently, to increased transistor densities and complexity of integrated circuits. With decreased geometries other processes and device parameters are scaled accordingly, including a supply voltage. No doubt, the low-voltage deep-submicron design adds new challenges to VLSI circuit testing. Thus, new alternative test methods have to be defined. Taking all those facts into account, a low-voltage, high-speed, and high-resolution current sensing circuitry is required to perform on-chip supply current monitoring.

In this paper, the feasibility of a fast I_{DDX} current monitor for testing of low-voltage submicron digital as well as mixed-signal circuits is verified. The monitor is capable of sensitive detecting of open and short faults at significantly higher speeds than current monitors previously reported [1-4].

2. Design of an On-chip Current Monitor

The fast built-in current monitor for concurrent I_{DDQ} and I_{DDT} measurement is described. The basic idea was to implement advantages of both current test techniques and to augment the testing capabilities of the current monitor.
The developed dual-resistor based current monitor (DRCM) consists of two resistors Rp and Rn, a current mirror, sensing and switching circuitry and a fast A/D converter. The monitor design is shown in Fig 1. The power supply current drawn by the CUT produces voltage drops across the resistors. The voltage drop across Rp makes the current mirror unbalanced that results in an output current. This mirrored current passes through the diode and charges the capacitor C to the voltage Vc. This way, the current signal is converted to the voltage signal.

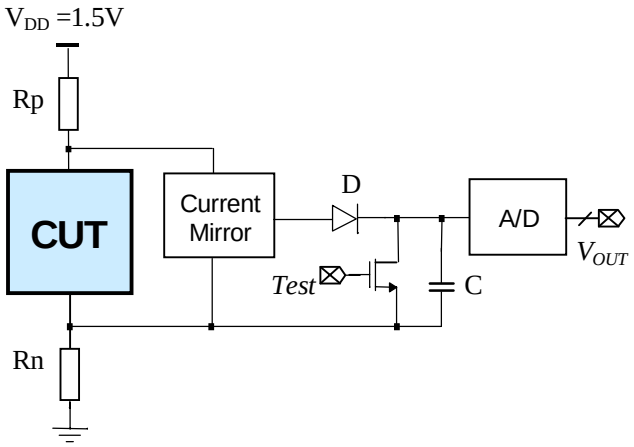

Figure 1 Dual-Resistor Current Monitor (DRCM)

After the sampling, a short pulse of the Test signal is applied to discharge the capacitor and to prepare it for the next sampling. The diode has an important function of cutting the reversing current signal off, when the current drops at the end of the pulse. The sampled Vc is further digitized using a fast A/D converter. The final result of an I_{DD} current conversion is a digital voltage easy to process and to evaluate. The value of the capacitor is allowed to be very small (less than 0.5pF) that enables very short charging and discharging time.

3. Achieved Results

The efficiency and sensitivity of the I_{DDX} monitor were verified on several experimental circuits. Two circuits were designed and used as CUT in order to verify a feasibility of the proposed current monitoring scheme for testing of real low-voltage CMOS circuits. For that purpose, both digital as well as mixed-signal circuit were selected. An *8x8 digital multiplier* was developed as the digital test vehicle that contains a short fault injected in it. Fig. 2 and Fig. 3 display the results of the scheme monitoring the multiplier supply current response for its fault-free and faulty operation, respectively. Waveforms from bottom to top: the original supply current drawn by the CUT, and the proportional voltage values measured by the monitor.

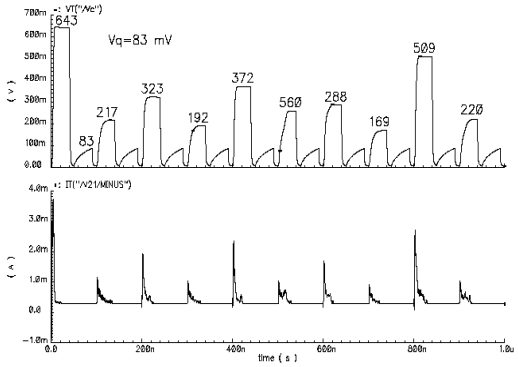

Figure 2 Fault-free multiplier response

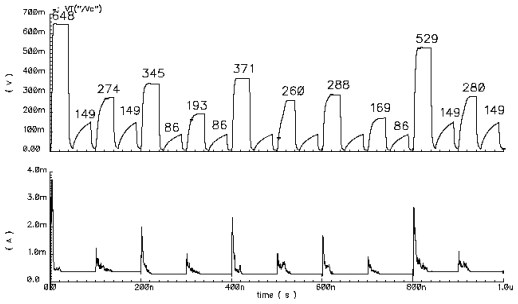

Figure 3 Multiplier response in a presence of a shot fault

The effect of the fault injection is shown in the above figures. During the first and the last periods of an input signal (0-200ns and 800n-1μs), a faulty current is added to the fault–free supply current in quiescent state. This elevated quiescent current of 450μA is monitored by the DRCM. Another design developed for the monitor evaluation was a mixed-signal circuit consisting of an A/D converter and a 4-bit multiplier connected to the output of the converter. For this circuit, the input stimulus of a pulse sequence 0-1.5 V at the frequency of 1MHz was used. Convenient detection of a short fault was observed as well.

4. Physical Implementation

The developed current monitor was implemented together with the digital CUT and fabricated in n-well 0.35μm CMOS technology. Fig. 4 depicts the core layout of the test chip. The CUT situated in the lower part of the layout occupies 45,900 μm^2. The area of the whole current monitor, seated in the upper part of the design, is 8,340 μm^2 that corresponds to 18 % of the total chip area.

The prototyped test chips were evaluated by a number of measurements. The input signal frequency and frequency of the control signal TEST were tuned in order to evaluate the monitor's maximum operating speed. It was found that monitor is able to operate at the maximum speed of 1MHz. However, more sophisticated measurement equipment eliminating the parasitics could help in obtaining better evaluation results. A possible influence of power supply deviations on the monitor performance was investigated as well. It has been proven the monitor circuit operates accurately for power supplies in a range from 1.46V to 2.1V (typical power supply of 1.5V).

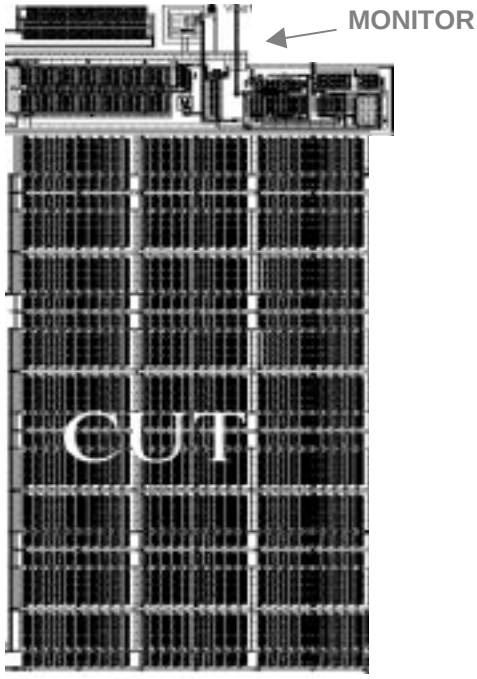

Figure 4 Layout of the monitor with a digital CUT

5. Conclusions

A practical on-chip high-speed high-resolution current monitoring circuit suitable for IDDX testing of low-voltage deep-submicron digital as well as mixed-signal circuits is proposed. The presented monitor is capable of monitoring either quiescent or transient part of the supply current response by a selection of the proper window of the monitored current. This is done using an external control signal (Test). The feasibility of the fast current monitor for testing of low-voltage submicron digital and mixed-signal circuits was verified on a number of the experimental designs. Furthermore, it is capable of sensitive detecting of open and short faults at significantly higher speed than current monitors previously developed.

References

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