A Tool for Fault Extraction in PCBs

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Abstract

This paper discusses testability problems in printed circuit boards. Current assembly technologies allow for an increased number of interconnections, thus requiring larger test sets to assure production quality. Besides simple boards, testing for all PCB possible faults at the production test stage is too expensive, so reduced test sets must be used. The extraction of realistic faults and inductive fault analysis allow reducing the number of faults to be tested by discarding those that are less likely to occur. These methods play a major role in a software tool for fault extraction in printed circuit boards, which is part of a system for testability analysis and planning of printed circuit boards.

1. Introduction

The Printed Circuit Board (PCB) remains the main support to connect electronic devices. The technology used in the design and fabrication of PCBs is directly associated to the development of Integrated Circuit (IC) packaging technology. Todays' components reduced dimensions allow for an increased interconnection density in PCBs [1].

Increasing the number of interconnections in a PCB usually means that more tests are needed and a larger number of nodes must be accessed to assure production quality. There is a cost associated both to the time consumed in those additional tests and to the overhead in extra circuitry to provide access to the desired test nodes. This gives a good reason to study methods that can increase the effectiveness of production tests, by making them defect-oriented, thus detecting the most probable defects introduced in the fabrication process and therefore minimising the number of tests and the number of nodes to be made accessible.

Section 2 presents fault extraction methods that select a set of faults to be tested by discarding faults with low probability of occurrence. These methods were implemented in a software tool that is described in section 3. Section 4 summarises the main conclusions and planned future developments.

2. Fault extraction methods

The defect spectrum in PCBs is clearly dominated by shorts and opens, although sources of defects vary from a fabrication process to another, and fault probabilities are also conditioned by tracks' width, length and proximity.

The extraction of realistic faults (ERF) is a method that uses information on the PCB layout to extract physically likely to occur faults [2]. The method uses track width, length and position, as well as pin position and size, to calculate distances between tracks and between pins. Assuming that defects causing shorts have a specified maximum size, we can determine all tracks and pins that can be shorted by this type of defect from the distances between tracks and between pins

Inductive fault analysis (IFA) is a systematic method for determining what faults are more likely to occur in a circuit [3]. IFA combines circuit topology with statistical data of defects occurring in the fabrication process. In the first step the defects are generated accordingly to statistical data and then the PCB schematic is checked to extract the resulting faults. These faults are then classified by type and probability of occurrence.

These two fault extraction methods, ERF and IFA, were used to build a program that performs fault extraction and offers a visualisation window, in which several PCB elements (tracks, pins, and components) can be shown and hidden according to convenience. Defects and faults can also be displayed overlapping the PCB layout for a better evaluation of results.

3. The tool for fault extraction in PCBs

The tool uses two major information sources that are needed to perform fault extraction:

- A file with the PCB layout description, generated by a CAD program for PCB design.
- The defect spectrum for a specified fabrication process. Two types of circular-shaped defects are currently supported: conductive material (causes shorts) and non-conductive material (causes opens). Other types of defects can be added as well.

One of two modes can be used for fault extraction: extraction of realistic faults or inductive fault analysis.

3.1 Extraction of realistic faults

In this mode, only geometrical characteristics of the board are considered. The user can specify the maximum defect size, so that only those tracks and pins that are within that limit can be expected to be shorted. However, this method is not useful in obtaining a classified list of faults because it considers minimum distances only. To cope with this problem, the algorithm was upgraded to include the calculation of critical areas which is used as a measure of likelihood of a short fault. The tool also calculates track width and length, and extracts open faults in tracks having a ratio length/width above a specified value.

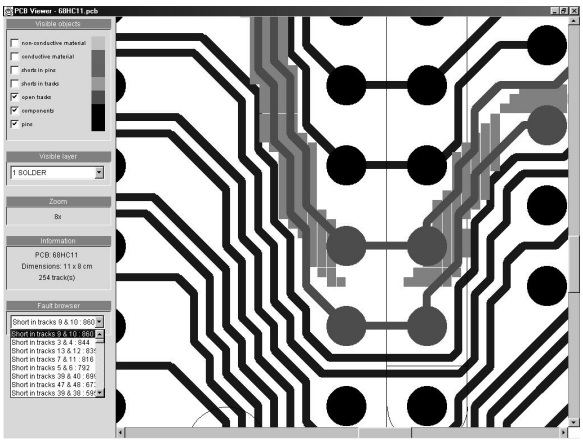

Figure 1: Critical area for shorts in two specified tracks.

3.2 Inductive fault analysis

In this mode the tool makes use of both the geometrical characteristics of the board and the defect spectrum of the fabrication process. After generating defects according to their statistical characteristics, the tool calculates minimum distances between defects and all tracks and pins. If two tracks (pins) are in contact with a defect of type "conductive material" then a short circuit between those tracks (pins) is extracted. If a defect of type "non-conductive material" is fully interrupting a track, an open fault is extracted on that track.

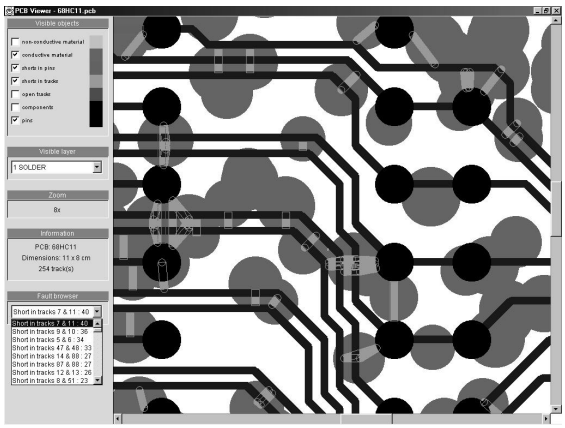

Figure 2: Extraction of shorts in tracks.

4. Conclusions and future developments

The tool for fault extraction in PCBs helps filling the gap between design and production stages, providing a better insight into the impact that the production process will have in test. It gives a feedback that can be used both in the design stage, by indicating the most critical regions of the design, and in the production stage, by helping in choosing a smaller and better test set, without diminishing the defect coverage.

The modular construction makes room for future enhancements that include a more detailed modelling of the fabrication defect spectrum and the inclusion of testability analysis at higher levels. More information on this work can be found in [4].

5. Acknowledgements

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6. References

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