Mixed-Signal Core-Based Testing

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Abstract

Core-based testing is an emerging test approach for systems-on-chip (SoC). At this early stage, the attention in core-based testing is restricted to digital cores. However, SoC often also contain mixed-signal and analog cores. In this paper, a new architecture for mixed-signal SoC testing is proposed employing a wrapper cell structure and an analog test bus, which provide the test access to the embedded cores in SoC. As an example, the analog front-end of a SoC including the new test hardware was evaluated by means of simulation.

1: Introduction

Core-based testing, which is described by the proposed IEEE standard P1500 [1], is an effective test method for Systems-on-Chip (SoC) consisting of digital embedded cores only. In this paper, the ideas developed in IEEE P1500 are extended for embedded analog/mixed-signal cores. A defect-oriented testing (DOT) approach is used for local test generation of each stand-alone analog core [2]. A concept for a structural test-access mechanism for embedded analog cores is proposed. This architecture is capable to transport test stimuli from the external IC inputs to the inputs of the core under test and subsequently route the test response from the core under test to the external IC outputs.

2: Proposed architecture

The proposed mixed-signal core-based testing architecture is depicted in Fig. 1. Compared to the standard P1500 architecture, the user-defined test access mechanism is extended with an analog test bus and the standard P1500 serial access controller is enhanced with an analog test bus controller part. Test control lines are present to the analog test bus and analog wrapper cells.

The wrapper cells used in our architecture include digital wrapper cells and analog wrapper cells [3], which carry digital and analog signals respectively. The digital input and output wrapper cells are identical to the ones suggested within P1500 [1]. The analog input and output wrapper cells, in which the basic components are analog switches [3], are connected to analog test busses. The Wrapper Control Interface (WCI) controls both the analog as well as the digital wrapper cells. For simplicity, the test-control lines are drawn as single lines.

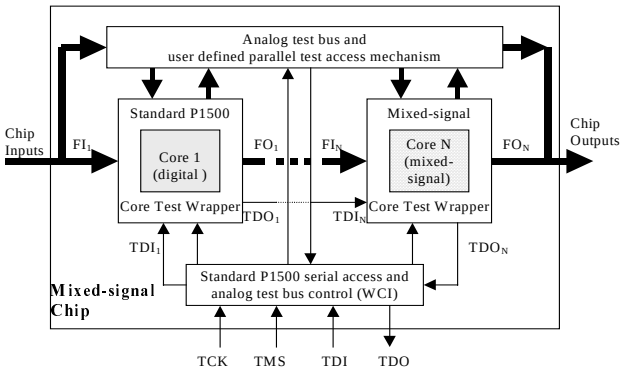

Fig. 1: Proposed architecture of mixed-signal core-based testing.

3: Example circuit and simulation results

In order to verify the new test architecture and the wrapper cells, an experiment was carried out on part of a locally designed system-on-chip [4]. The considered embedded core is a Programmable Gain Amplifier (PGA), having an analog input and output and a digital input, which controls the gain. Hence an analog input and output wrapper cell and a digital input wrapper cell surround the core. A low-pass filter (LPF) precedes the embedded analog core, while a VI converter (VIC) succeeds it. This part of the set-up of the SoC is shown in Fig. 2. For simplicity, the other cores in the SoC have been clustered. The Analog Input and Analog Output Test Busses are denoted AITB and AOTB. PIA and POA denote analog primary inputs and outputs, while PID and

POD are their digital counterparts.

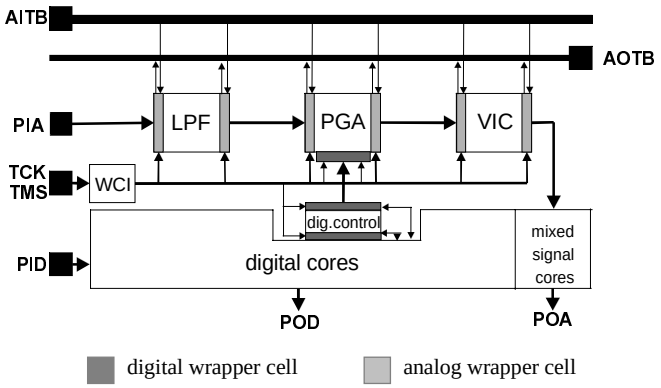

Fig. 2: Part of the system with embedded cores.

In our approach, a structural/defect-oriented test-signal generation program [5] is employed to generate the test signal for the stand-alone PGA. The most sensitive tests have been selected by the program, e.g. using the least detectable impact of a bridging fault (=bridging resistance value) as a criterion. Subsequently, fault clustering/collapsing reduces the number of test signals.

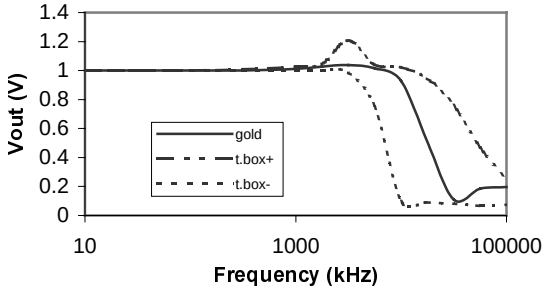

Fig. 3: Output frequency characteristics of PGA with tolerance box for AC testing.

To obtain acceptable responses we have produced a tolerance box by using Monte Carlo simulation. For the process-induced tolerances for real industrial process realistic values are assumed. The output frequency characteristics of the PGA with tolerance boxes are given in Fig. 3.

Afterwards, the previously derived structural tests of the stand-alone core have been used as a basis for testing the embedded PGA using our mixed-signal core-based testing approach. Because of the limited length of the paper, only one AC test is shown in Fig. 4. A mixed-level description (transistor level /logic-gate level /Verilog-A behavioral level) of the embedded structure as shown in Fig. 2 has been simulated using Cadence Analog Artist.

In Fig. 4, a high frequency test signal is used to test a single bridging fault. The results show that the high frequency output signal is degraded when it is transported from PGA output to AOTB through the analog test bus and switches in wrapper cells. However, although the signals are degraded, we can still detect the fault at AOTB since there is a substantial difference between the output of the fault-free circuit and faulty circuit, which means the detectable fault at PGA output can also be detected at AOTB.

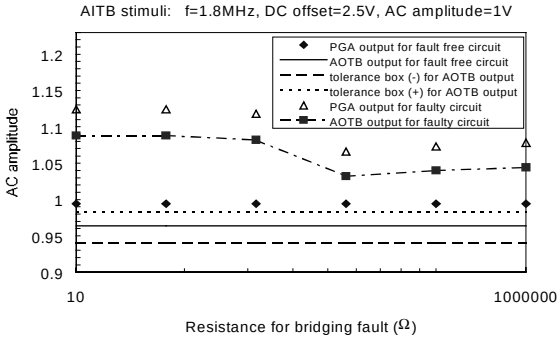

Fig. 4: AC test (high frequency) simulation results showing AC stimuli at AITB, AC amplitude of PGA output and AOTB under various bridging fault conditions.

4: Conclusions

A new architecture for testing mixed-signal SoC has been proposed based on embedded core-based testing principles. Wrapper cell structures and analog test buses have been used to provide the test access for the embedded cores. As an example, an embedded mixed-signal core, a programmable gain amplifier, has been used to show the viability of the concept.

5: Acknowledgement

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References

[1] IEEE Website, http://grouper.ieee.org/groups/1500/.
[2] Y.Xing, " Defect-Oriented Testing of Mixed-Signal ICs: Some Industrial Experience", in Proc. ITC, 1998, pp. 678-687.
[3] M. Stancic, L. Fang and H. G. Kerkhoff, "Analogue Core-Based Test-Pattern Generation, " Proc. of ProRISC99, November 1999, Mierlo, pp. 461-466.
[4] R. Tangelder, G. Dienmel and H. Kerkhoff, " Smart Sensor Application: An Integrated Compass", Proc. IEEE European Design & Test Conference, 1997, pp. 195-199.
[5] V. Kaal and H. Kerkhoff, " Compact Structural Test Generation for Analog Macros", Proc. IEEE European Design and Test Conference, 1997, pp. 581-587.