An On-Line BIST Structure for Distributed Control Systems

Liviu Miclea, Dan Cimpoca, Mihaela Gordan
Technical University of Cluj-Napoca
26-28 Baritiu Street, RO-3400 Cluj-Napoca, Romania
Tel. +40 64 193161 ext. 141, Fax. +40 64 192055
E-mail: Liviu.Miclea@aut.utcluj.ro, Dan.Cimpoca@aut.utcluj.ro, Mihaela.Gordan@bel.utcluj.ro

Abstract

The present paper proposes a structure, aiming at overcoming the problems that arise during on-line testing of distributed control systems. This structure is a flexible architecture allowing activating and controlling different BIST tests at different levels of hierarchy in the distributed systems.

1: Introduction

A major trend in testing and qualitative control activity is the use of Information Technology. New approaches have appeared, correspondingly to this trend: development of design techniques for automated testing, development of testing techniques for distributed systems, increase of discrete critical systems availability by providing for fault tolerance, systems' diagnosis using visual inspection. These approaches materialize in the appearance of new equipment manufactured according to new concepts.

Distributed systems have become a common presence in the area of control systems. In most of the cases, the communication media and the devices that compose a distributed system support virtually simultaneous transfer and processing of data blocks that belong to independent logical processes. This idea suggested us that it would be possible to extend the original functions of distributed systems with testing facilities.

Control functions and testing facilities form two logically independent blocks, which overlap. The problem of testing distributed control systems is a critical one, because testing cannot interrupt control actions. Yet, testing the system is very important, because a failure may occur at any time (especially if the system works in a rough environment). This is why testing and control must be concurrent activities.

An approach to performance testing in Multi Chip modules has been defined in [2]. It is based on an architecture, where the standard Boundary Scan path can be reconfigured in a BIST structure that allows pseudo random pattern generation and signature compaction. The proposed solution is based on the modification of the standard Boundary Scan cell.

The paper [1] proposes SHD-BIST (System-level Hierarchical Distributed BIST), a BIST control methodology of an hierarchical system, allowing activating and controlling different tests at different levels of hierarchy with a minimum overhead in terms of area and test time.

Despite their novelty, none of the mentioned approaches are particularly devoted to solving the problem of distributed control systems' on-line testing.

Our paper proposes a structure, aiming at solving the problem of the distributed control systems' on-line testing.

2: Proposed technique

We propose a structure (see Figure 1) where a testing module is attached to each component of the distributed system. We distinguish between master and slave testing modules.

Master testing module is a software module. As its name suggests, it will play the role of master in testing activity. It has two major jobs to accomplish: the first is to test and verify master device regular activity, and the second is to lead testing activity in slave device and to gather resulting data.

Slave testing module is a mixed module: it consists of a hardware side and a software side. We will try to take advantage of the fact that almost all programmable components manufactured today comply with boundary

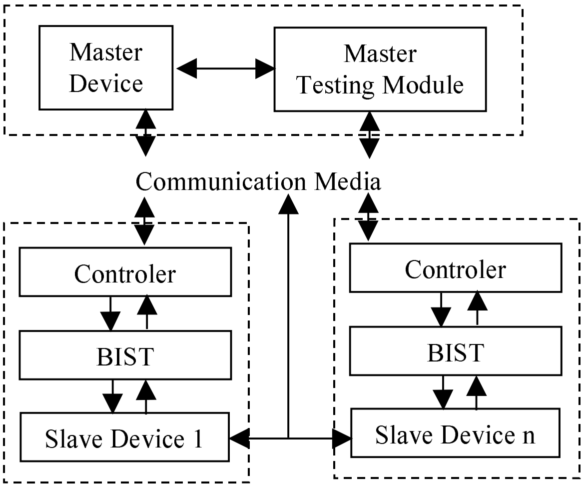

Fig. 1. Proposed structure

scan architecture. Hardware side is based on boundary scan architecture, with an extension that makes this architecture re-configurable, so that it can be used for on-line testing. Software side of the slave module (that implements the test controller) will use existent communications driver modules that are part of the initial system. Slave testing module has two activities: first of them is to communicate with master testing module (that is, to receive commands and test vectors for external test, and to send back test results), and second is to co-ordinate testing of slave device according to the commands received. This slave testing module must be implemented by hardware, in case of non-intelligent slave devices.

The proposed re-configurable structure to allow on-line interconnect performance testing is based on an enhancement to the IEEE 1149.1 architecture. This enhancement allows each boundary-scan cell to accomplish two new functions, in addition to its normal functions. These new functions are: TEST_INT_Active, where the cell is a component of a LFSR register, and TEST_INT_Transparent, where the cell in transparent to the current interconnect testing.

3: Results

The proposed BIST structure is able to carry on slave and master devices testing, as well as test information (test vectors, test results) transfer among slave and master devices. Devices testing is based on the following test instructions: NET_EXTEST - that coordinates interconnect testing using reconfigurable BS logic, NET_RUNBIST – that executes BIST for a component, and NET_INTEST – that coordinates in-test for non-BIST-ed components, in off-line mode. Execution of a test can be triggered by local or remote events (such as

Fault latency in the proposed structure is variable, and depends on how often tests are performed, and results transmitted to master. The operator is in control of these parameters. If a test is performed too often, fault latency is low, but normal operation of that device might be affected. Sending large test results too often over the communications media would also affect network loading.

The distributed testing system has a modular structure, consisting of two layers: the Testing Layer and the Communications Layer. Components of each layer consist of groups of functions and structures, which are exported and made available to the entire distributed system. That is, a device can call a function from “Testing functions” group, for instance, in a slave device, and get testing results.

High-level functions from Testing Layer can call low-level functions from Communications Layer, to send test results to another device. Alternatively, remote testing is triggered by a call to a Command Function (Communications Layer), that call then one of the Testing Functions (Testing Layer). Thus, there is a two-way communication between the layers.

We have used DCOM (Distributed Component Object Model) and RPC (Remote Procedure Call) to implement Communications Layer, in the case of a PC network. Communications Layer is implemented as a software component.

4: Conclusions and Future Work

A technique for testing distributed control systems, based on re-configurable boundary-scan cell, BIST techniques and software component technologies has been presented with the aim of getting on-line test capabilities for this kind of systems.

We are now working in the implementation of the Testing Layer. We also conduct our efforts towards an implementation of the hardware and software modules, which is expected to increase distributed control systems' availability.

5: References

1. A. Benso, S. Chiusano, P. Prinetto, Y. Zorian, *A Distributed BIST Manager for Hierarchical System Test and Diagnosis*, HLDVT'98 Proceedings
2. B. Dervisoglu, M. Riccetti, B. Eklow, *Shared I/O-Cell Structure: A Framework for Extending the IEEE 1149.1 Boundary-Scan Standard*, International Test Conference 1998 Proceedings, pp. 980-989