A High Performance Low Power Scan Element

Luis Basto, Analog Devices
Dwight Galbi, Analog Devices

8901 N. Capital of Texas Hwy., Suite 1300, Austin, Tx 78759

Key Words: High performance, Low power, Scan, Design for Test

Abstract

Scan testing is a commonly used technology to achieve verifiable high fault coverage in digital designs. As design technology progresses into very deep submicron, enabling ever higher density and complexity, there is a need to develop storage elements that are high performance, low power, and testable. This paper describes a novel design that combines the properties of low power, high performance, and scannable flip-flops into a scannable dual edge pulse-triggered storage element.

Introduction

Design geometries continually shrink to achieve higher performance and density. As the complexity of these chips increases, scan testability becomes a necessity. However, it must be implemented with minimal impact to performance.

Research on high performance low power design leads to dual edge-triggered and pulse-triggered flip-flops. Pulse-triggered flip-flops are used in high performance designs because they allow for time borrowing to achieve maximum performance [1]. Dual edge-triggered designs can reduce overall chip power by reducing clock tree power by up to 50% [2,3]. LSSD [4] and multiplexed scan are the two most common scan techniques used to make designs testable. This paper describes a new flip-flop design for high performance, low power, and scan testability.

Implementation Details

As clock periods decrease in high performance designs, the cycle time becomes the critical design factor. Latch-based designs allow for time borrowing between logic stages. This often can balance the delay between two stages of logic to reach a higher performance target. However, in typical flip-flop based designs, time borrowing is not possible. Pulse triggered flip-flops can be used to solve this problem. They allow for some time borrowing and minimal propagation delay to achieve maximum performance, yet still maintain the characteristics of a flip-flop based design.

The key to saving power is in using both edges of the clock to capture data. In the common single edge-triggered design, data is captured on a single clock edge. In a dual edge-triggered design, data is captured on both clock edges allowing half the clock frequency with the same data rate, thereby saving power in the clock tree network by up to 50%. Since in high performance designs the clock network can consume up to 50% of the chip power, using dual edge-triggered designs can reduce overall chip power by up to 25%.

A schematic of a dual edge-triggered flip-flop is shown in Figure 1. It is composed of two storage elements in parallel, each clocked by opposite clock levels. Data is captured at every clock transition, effectively doubling the data rate, or conversely, the clock frequency can be halved for the same throughput.

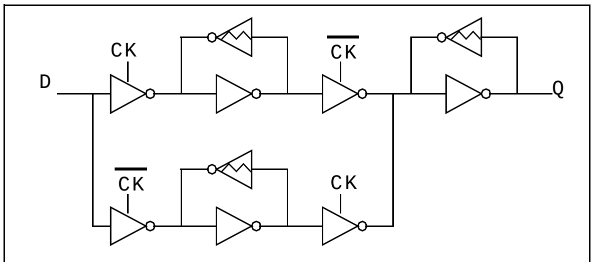

Figure 1: A dual edge-triggered flipflop

Combining both dual and pulse triggering produces a high performance, low power flip-flop design [5]. An example of this type of design is shown in Figure 2. The pulse generator circuit creates a short pulse for every clock transition, and this pulse is used as the capture clock in the flip-flop.

Using both edges of the clock is inherently a testability problem since one of the primary rules for scan design is to capture data on only one edge of the clock. A multiplexed scan version of the flip-flop can be used but will not be described since some performance is lost due to the extra delay of the multiplexor. The only scannable flip-flop that maintains the characteristics of low power and high performance is a level-sensitive scan design. In order to implement LSSD efficiently, a dual-edge, pulse triggered flip-flop must be used.

One such implementation is shown in Figure 3. In functional operation the scan clocks AK and BK are held off and the flip-flop operates normally. In scan shift mode, the system clock CK is held either high or low, which prevents any pulses from being generated and thus prevents the data input from entering the flip-flop. The shift clocks AK and BK are then pulsed successively to shift data during scan mode.

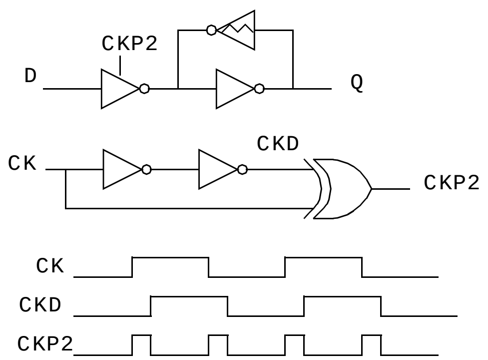

Figure 2: A dual-edge pulse-triggered FF

Simulation data

The design was simulated with hspice in a 0.18µm process. Simulation data shows operation of the flip-flop is possible with a range of pulse widths and performance trade-offs. The performance of this flip-flop in comparison with other types of flip-flops is shown in Table 1.

The available stage cycle time is the amount of time available for logic evaluation, which is basically the period minus the flight time through the flip-flop. This is shown as a percentage of the clock period. Single and dual-edge pulse flip-flops have identical characteristics except that the dual-edge version can save up to 50% power in the clock network.

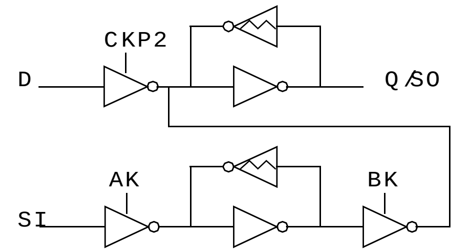

Figure 3: A scan implementation of a dual-edge pulse-triggered flip-flop

Conclusion

We have described a novel flip-flop design combining the benefits of pulse-triggered, dual edge-triggered, and testability into a single high performance, low power, scan element.

References

1. H. Partovi, et. al., "Flow-through latch and edge-triggered flip-flop hybrid elements", ISSCC Digest Tech. Papers, pp 138-139, Feb. 1996.
2. Razak Hossain, Laszek D. Wronski, Alexander Albicki, "Low Power Design Using Double Edge-Triggered Flip-Flop", IEEE Trans. on Very Large Scale Integration, pp 261-265, June 1994.
3. Rafael Peset Llopis and Manoj Sachdev, "Low Power, Testable Dual Edge Triggered Flip-Flops", pp. 341-345, ISPLED, 1996.
4. E.B. Eichelberger, T.W. Williams, "A Logic Design Structure for LSI Testing," Proc. 14th Design Automation Conference, pp. 462-468, 1977.
5. A.G.M. Strollo, E. Napoli, C. Cumino, "Low Poser Double Edge-triggered Flip-Flop Using One Latch", Electronic Letters, pp 187-188, Feb. 4, 1999.

Table 1: Performance data of different flip-flop designs

	#trans	#trans clkgen	Stage Cycle Time/Period*	Setup time	Hold time	Power	LSSD scannable
Single edge	16	4	80%	s	h	p	Yes
Dual edge	28	4	78%	s+d	h	1.7p	No
Pulse	8	12	90%	$s-t_p$	$h+t_p$	0.5p	Yes
Dual-edge pulse	8	12	90%	$s-t_p$	$h+t_p$	0.5p	Yes

* - based on 20 logic gates/cycle
d - added delay due to extra load on inputs
t_p - width of clock pulse to flip-flop