Partial Scan Design Based on Reachable States

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Abstract

Partial scan FF selection method based on reachable states is proposed as a design for testability of a sequential circuit, and its validity is evaluated. A reachable state is defined as a state which can be reached from an initial state by applying an input sequence to sequential circuit. Taking into account the relation between the scan FFs and the reachable states, scan FFs are selected to increase the number of reachable states. The experimental results of scan FF selection and test generation using ISCAS'89 benchmark circuits show that fault coverage and test efficiency reach 95% and 100%, respectively, when 20% of all FFs are scanned.
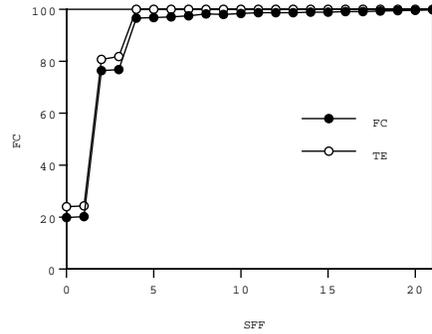
Figure 1: Fault coverage and test efficiency of s526 circuit.

1 Definitions

Some words used here are defined.

[Definition 1] (state) A state is a combination of FFs' logic values in sequential circuits. A state s is represented as $s = (v_0, v_1, \cdots, v_{n-1}) \in [0, 1]^n$, where v_i is the logic value of i-th FF.

[Definition 2] (reachable state) A reachable state is a state which is reachable from an initial state.

[Definition 3] (0-frequency, 1-frequency) The definitions of 0-frequency $F_0(i)$ and 1-frequency $F_1(i)$ of i-th FF are as follows.

Figure 2: Test generation time and test vector length of s526 circuit.

$$F_0(i) = |\{s|s \in S_r, v_i = 0\}|, \quad (1)$$

$$F_1(i) = |\{s|s \in S_r, v_i = 1\}|, \quad (2)$$
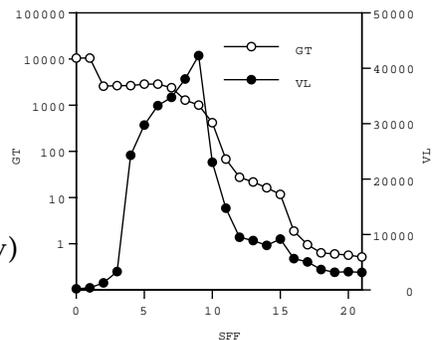
where S_r is the set of reachable states.

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Table 1: Results of test pattern generation and comparison with other method

circuit	# of FFs	proposed method	[1]	[2]
s298	14	3/98.1/100	1/94.8/100	10/99.4/100
s344	15	3/96.9/99.7	3/98.8/100	5/98.8/100
s349	15	3/96.3/100	3/98.3/100	4/98.3/100
s382	21	4/98.8/100	5/97.5/100	6/99.3/100
s386	6	2/95.3/100	2/92.2/100	4/100/100
s400	21	4/97.4/100	5/95.8/100	5/97.6/100
s420	16	11/94.9/100	-	16/100/100
s444	21	4/96.0/100	5/94.9/100	6/96.0/100
s510	6	4/99.3/100	5/100/100	3/99.3/100
s526	21	4/96.62/100	7/98.7/100	15/98.7/100
s641	19	4/99.4/100	5/94.2/100	7/99.4/100
s713	19	4/92.9/100	5/88.1/100	7/92.9/100
s820	5	2/100/100	2/100/100	2/100/100
s832	5	3/98.4/100	2/98.4/100	2/98.4/100
s838	32	27/97.4/100	-	29/53.7/99.9
s953	29	5/98.1/100	3/100/100	3/100/100
s1196	18	1/99.8/100	1/99.8/100	-
s1238	18	1/94.7/100	1/94.8/100	-
s1423	74	41/95.5/96.4	-	41/97.9/98.8
s1488	6	1/99.9/100	2/100/100	2/99.9/100
s1494	6	1/99.1/100	3/99.2/100	2/99.1/100
s5378	179	50/92.6/98.3	80/97.5/99.6	48/97.1/99.9

To maximize the lower limits of reachable state of scanned circuit, the FF satisfied the below condition is required to be scanned.

$$\max_{0 \le i \le n-1} |F_0(i) - F_1(i)|. \tag{3}$$

2 Test Pattern Generation Results

Test patterns are generated using HITEC [4]. The upper limit of backtrack is 100000.

References

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[4] T.M. Niermann and J.H. Patel, "HITEC: A Test Generation Package for Sequential Circuits," European Conf. on Design Automation, pp. 214–218, 1991.