# On the Acceleration of BST-based Monitoring Processes

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## Abstract

*Non-intrusive BST monitoring is a concurrent testing technique in which the operating vectors match the test patterns. This paper presents an enhancement to speedup pattern searching that reduces the average monitoring interval by several orders of magnitude, at the same time it improves the on-line fault-coverage.*

***Keywords:*** *Dependable VLSI, Concurrent testing, BST, DFT.*

## 1. Introduction

Integrated circuits find continuously new applications, one of the reasons being the low cost allowed by miniaturization. Geometry shrinking brings lower supply voltages and less power too, as well as higher operating frequencies. However, it also impacts circuit reliability, the small energy needed for commutations and the short noise margins leading to circuits that are more sensitive to noise influences, increasing the probability of temporary faults. A faster physical degradation may also lead to permanent faults [1].

To face these handicaps, applications expected to be dependable imply on-line tests, which can be *scheduled* or *concurrent*. In the first case, BIST or IEEE 1149.1 std based approaches are available to the designer [2, 3, 4], but these forced tests must be carefully applied in on-line operation since the higher activity induced by compact test sets may be dangerous and harmful to an already hot mission circuit. In the sub-micron technology, this activity may easily produce destructive hot-spots [5], leading to a growing interest for solutions not increasing the mission circuit activity, and concurrent testing is the ideal approach.

Traditional solutions in this area are *duplication with comparison* and *self-checking* designs, both presenting specific advantages and drawbacks. Recently, a concurrent monitoring technique based on the 1149.1 infrastructure joined the above options. As showed in [6], a slightly enhanced BST infrastructure searches matches between the input operation vectors and each reference pattern of the test set for the specified fault coverage.

This paper presents an evolution of the above technique, named Concurrent Scan Test (**CST**), which allows searching multiple binary combinations of each uploaded test pattern.

## 2. Background

Concurrent testing has four major advantages:

1. Errors are detected immediately or, at least, in shorter intervals than through scheduled tests.
2. No need to suspend, or reset, the mission circuit operation if there is no errors.
3. Lower requirements to fault models and to the fault-coverage test.
4. No need to consider delay fault models.

The first point is justified by the intervals between scheduled tests, which can not be too frequent. The second assertion is obvious and avoids dangerous reintegration processes. Concerning the third, it was shown that monitoring the circuit operation may improve the fault detection ability of a set of patterns, by 10% or more of its estimated fault-coverage [7]. This aspect, also noticed by many BIST supporters, can be justified in part because a wider number of applied patterns seems to be more effective than very compact test sets usually found in the pure BST approaches (equal estimated fault coverage both). Delay and propagation faults need only to be considered during design phase and, eventually, low speed tests, but the errors generated by such kind of faults will be easily detected with concurrent mechanisms.

The base approach to concurrent monitoring through the BST infrastructure was presented in [6]. As shown in figure 1, the input scan cells store the bits of a test vector ($\mathbf{VT_i}$) and, upon an input match ($\mathbf{V_i} = \mathbf{VT_i}$) the output scan cells will be triggered by the control unit to capture (or check) the corresponding output pattern ($\mathbf{V_o}$).

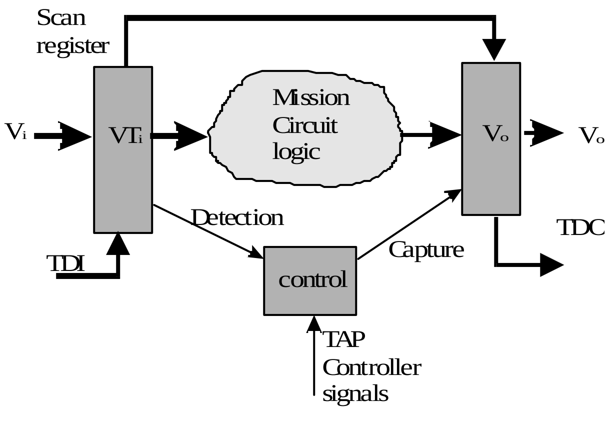

**Figure 1. Concurrent scan monitoring principle**

## The accelerating principle

The input scan cells in the above scheme are able to store a single bit, allowing to search one (only) **$VT_i$** at a time. Every input vector matching $VT_i$ will be detected, until a new reference pattern is scanned into the cell storage latch, updating the search.

To reduce the *latency* interval, a faster search requires seeking multiple vectors and the CST evolution is able to search the reference pattern plus its binary complement. This way, an uploaded $VT_i$ drives the search of two (complementary) vectors, or **co-vectors**, with two immediate consequences:

- The average matching time is reduce, to one half.
- The on-line fault-coverage will be estimated from the reunion of the sets of faults detected by each vector.

A further improvement is to divide $VT_i$ in two parts, allowing to search simultaneous and independently each part and its binary complement. In this case, each $VT_i$ drives the search of four patterns at a time, leading to a new division of the average matching time and to an higher fault-coverage. Pushing the division process, figure 2 shows an example with the input partitioned into 4 parts (**P0-3**), to search 16 co-vectors at a time.

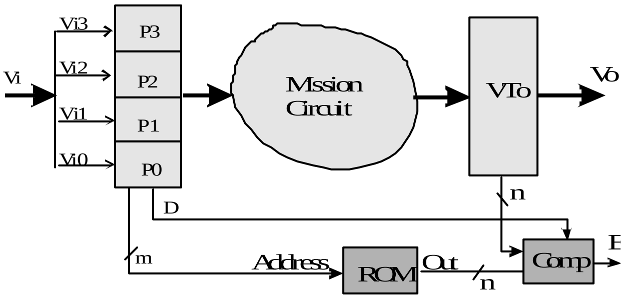

**Figure 2. The CST principle**

The input match occurs inside the scan cells and generates two signals:

**- Address** : these **m** lines, equaling the number of parts (m=4 in the example), select the expected response in the ROM memory, either the complete output word or a space compaction of it. In case of non partition, a single line distinguishes $VT_i$ from its binary compliment.

- **D** : the *detection* signal, enabling the **Comp**arator to generate the **E**rror signal while the match is present.

Beyond accelerating the monitoring process, another relevant enhancement arises from this approach: the number of test patterns to store is reduced, avoiding those detecting faults covered by co-vectors of previously defined patterns, which may lead to a very small number of explicit test patterns.

We must emphasize that a division of $VT_i$ in four parts enhances the average matching interval by more than one order of magnitude. Wide input patterns may be divided in 10 (or more) parts, to seek 1K co-vectors and provide over three orders of magnitude shorter latency intervals.

## Comments and results

First of all it must be noticed that the flexibility of the 1149.1 infrastructure, allowing to insert scan cells in the test points that are harder to control and/or observe, simplifies Test Pattern Generation (ATPG) at the same time the test set can be minimized. The number of test patterns is a relevant parameter in this technique, because the higher this number the wider will be the average monitoring interval.

A second relevant aspect to point in this technique is to let mission circuit untouched, the monitoring process being performed at the input and output nodes (scan cells) only. In addition, the IEEE 1149.1 infrastructure has been also improved to become dependable enough in concurrent operation as shown in [8], through a parity bit allowing to check scan data integrity, which is transparent to the IEEE standard.

Concerning practical results, the division of $VT_i$ up to 8 parts was implemented to search 256 combinations simultaneously and, to satisfy dependability needs, was elected a space compaction scheme with a parity bit for each 4 output bits. To calculate the ROM size, supposing the example with 16 $VT_i$ plus 15 co-vectors of each, we find 16*16*4=1Kbit. This value can be still reduced to 256 bits, if a single parity bit of the whole output word satisfies dependability specs.

Tools to define the optimum approach are currently being developed, but results so far obtained show a speed improvement from 2 up to 1K and more, together with a ROM reduction to about 30% of the size needed in the case of a non-partition scheme.

## Selected Papers

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