ATPG for I_{DDQ} and/or Voltage Testing of Combinational Circuits Using an Arbitrary Fault Library for Basic Gates

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Abstract

The paper and poster deal with the Automatic Test Pattern Generation (ATPG) system named DefGen running over an arbitrary fault library for every basic gate in a tested circuit. A test set can be generated for voltage and/or I_{DDQ} testing for faults and patterns specified in the fault library. Some experiments have been done on the ISCAS'85 benchmark circuits using two types of fault libraries.

1 DefGen – ATPG system for I_{DDQ} and/or voltage testing

Each physical defect should be covered by the test method that leads to the lowest overall testing costs, taking into account e.g. the complexity of test generation, and the test application time. Certain types of CMOS defects are detected either by current or by voltage test patterns and the other ones by both patterns [1]. Current testing was found to be useful for testing of CMOS circuits because it can detect a large class of manufacturing defects: stuck-at, shorts, bridges, opens. Some of test generation techniques for I_{DDQ} testing have been published (e.g. [2]) or classical Automatic Test Pattern Generation (ATPG) systems have been extended by generation of I_{DDQ} test patterns.

The presented system named DefGen contributes to the ATPG systems with the novelty to generate tests in accordance with user's requirements for patterns and faults. The DefGen system consists of several TPG and fault simulation tools [3,4] implemented in user-friendly graphical interface. The TPG techniques are based on the implicit fault model. Thus, some test patterns are defined for every basic gate (NAND, AND, OR, NOR, NOT, EXOR, EXNOR, BUFF) which should be covered by input patterns. A list of patterns created for every gate is named "fault conditions" for the gate, and is included in the fault conditions library. The TPG tools can generate a test set over an arbitrary list of fault conditions for every gate with respect to user's requirements. A fault localisation algorithm (*LocGen*) has been added to the ATPG system based on an analysis of fault tables. The fault tables determine the coverage of individual faults that are detected by corresponding voltage and/or current patterns (received e.g. from electrical simulation for different defects). These ones are created for every gate and they form a fault library that can be also modified or created by the user.

Two TPG techniques are implemented in the DefGen system: random (*RndGen*) and deterministic (*DetGen)* ones running together with a fault simulator. The fault simulator (*FaultSim)* runs also separately, for external input patterns consist of three values: 0,1 and don't care value. The deterministic technique is based on FAN strategies, and the deductive fault simulation technique is implemented in FaultSim. Generally, the DefGen system can generate the optimum test set, depending on the constraints given for the used fault library, which contains data regarding the detection and the localisation of the faults considered for the basic gates. The accepted circuit description is the language used for the ISCAS'85 circuits or the EDIF format (ISCAS'85 – EDIF interface is included in DefGen).

The test generation process is split into two phases. The first one is fault detection and the reported fault coverage is represented by the fault conditions coverage. The second one is aimed at fault localisation according to the used fault library, and the real fault coverage is computed.

2 Experimental results

Experiments on ISCAS'85 benchmark circuits have been done using two different fault conditions and fault libraries (they were made under the Copernicus project CP940391: Unified Built-In Self Test Approach for Full Defect Testing in Mixed Electronic Devices). The following types of faults have been considered there at the structural level:

- stuck-at, stuck-off, stuck-on faults
- intra-gate shorts (transistor shorts between terminals of a transistor).

An example of one fault library (two tables) for NAND2 is introduced in Tab.1. Results from electrical simulation using voltage and current measurements for the exhaustive test set for the gate are involved. The value 1 (0) indicates that the fault can be detected (undetected) by corresponding pattern. The list of investigated faults is on the top of the tables. The similar tables have been used for every basic gate. The results from the both phases of test pattern generation on ISCAS'85 benchmark circuits are reported in Tab.2. These results have not been compared with other TPG tools.

Table 1: Voltage and current fault libraries for NAND2

	Voltage fault library	a/0	a/1	b/0	b/1	y/0	y/1	mp1off	mp2off	mn1off	mn2off	mp1on	mp2on	mn1on	mn2on	mp1gds	mp2gds	mn1gds	mn2gds	mn1dss	mn2dss
0	00/1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0
1	01/1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0
2	10/1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1
3	11/0	1	0	1	0	0	1	0	0	1	1	0	0	0	0	1	1	1	1	0	0
	Current fault library	a/0	a/1	b/0	b/1	y/0	y/1	mp1off	mp2off	mn1off	mn2off	mp1on	mp2on	mn1on	mn2on	mp1gds	mp2gds	mn1gds	mn2gds	mn1dss	mn2dss
0	00/1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0
1	01/1	0	0	0	0	1	0	0	0	0	0	0	0	1	0	1	0	0	0	1	0
2	10/1	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1
3	11/0	0	0	0	0	0	1	0	0	0	0	1	1	0	0	0	0	0	0	0	0

Table 2: Results from the DefGen system for ISCAS'85 benchmark circuits

ISCAS '85	**N° of effective vectors**	**N° of current tests**	**N° of voltage tests**	**N° of current+ voltage tests**	**Time [h:m:s]**	**Fault condition coverage [%]**	**N° of defectable faults**	**N° of uncovered faults**	**N° of aborted faults**	**Fault coverage [%]**
C432	84	2	47	35	0:00:27	95,28	2478	55	18	97,78
C499	197	66	48	83	0:00:05	99,44	3924	8	0	99,80
C880	81	1	66	14	0:00:07	100,00	6918	0	0	100,00
C1355	132	4	46	82	0:00:08	99,75	9700	8	0	99,92
C1908	179	5	59	115	0:01:23	99,73	13460	11	6	99,92
C2670	131	7	96	28	0:18:18	96,94	19354	353	105	98,17
C3540	182	5	141	36	0:15:14	97,09	27646	432	31	98,47
C5315	237	1	206	30	0:08:14	99,16	34982	144	73	99,59
C2688	55	1	39	15	0:34:43	99,27	41024	191	20	99,53
C7552	181	1	142	38	0:43:29	98,75	58700	369	56	99,37

3 Conclusion

The DefGen ATPG system has been imlemented in Visual C++. Some experiments performed on ISCAS'85 benchmark circuits show flexibility and functionality of the DefGen system. The work has been supported by the CP977133 project: Microelectronic virtual laboratory for co-operating in research and knowledge transfer and by the VEGA 2/6091/99 project: Behavioural and real defects oriented test generation for digital circuits and systems.

References

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