# A Non-Scan Testable Design of Sequential Circuits

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**Abstract**

The testable design can be implemented by enhancing controllability and observability. This paper discusses a non-scan testable design for a sequential circuit by only focusing the improvement of controllability. The proposed design modifies a circuit so that all the FFs can be directly controlled by primary inputs in a test mode. Experimental results show that testability can be improved by this method.

## 1. Introduction

As a method for testing a sequential circuit efficiently, a scan design is usually used. This design has the following drawbacks:1) testing time is long, 2) at-speed test cannot be performed. Hence, we should discuss a non-scan testable design for a sequential circuit[1][2].

In order to make a logic circuit be testable, controllability and/or observability should be enhanced using some design modification. In this paper, we consider that the controllability has more effect on the testability than the observability and discuss a non-scan testable design for a sequential circuit by only focusing the improvement of controllability. The proposed design modifies a circuit so that all the FFs can be directly controlled by primary inputs in a test mode. Experimental results show that we can get a good testability using this method.

## 2. Non-scan testable design 1

The number of primary inputs is defined as N_PI. The number of FFs is defined as N_FF. Firstly, we discuss the case that N_PI is less than or equal to N_FF.

In order to make a sequential circuit be controllable, we modify the circuit as shown in Fig.1. A pseudo output and a primary input are inputted to a multiplexer(MUX). TEST is a selection input of a MUX. TEST is fixed to 0 in a normal operation mode and a pseudo output is fed to a FF. In a test mode, TEST is controlled by a test pattern, and a pseudo output is sometimes fed to a FF and a primary input is sometimes fed to a FF. This modification makes it possible not only that a FF is set to an arbitrary value from a primary input but also that the fault information propagated at a pseudo output can be propagated further to a combinational circuit.

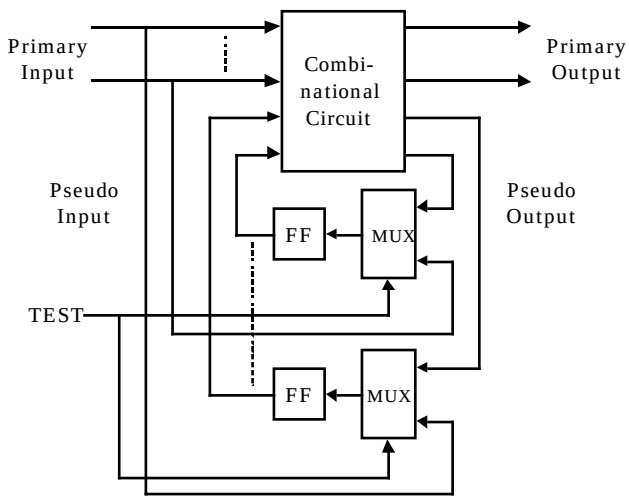


**Fig.1 Circuit modification -1**

## 3. Non-scan testable design 2

### 3.1 Equivalent group of FFs

The above discussed method has the problem that if N_PI < N_FF, all the FFs cannot be directly controlled by primary inputs. To meet with this problem, we discuss the method that some FFs are controlled by one primary input.
[Definition 1]

We consider all the test patterns for a combinational circuit part of a sequential circuit. $FF_i$ and $FF_j$ are called to be equivalent to each other, iff the same logic value can always be assigned to $FF_i$ and $FF_j$ by appropriately setting a logic value 0 or 1 to a don't care value in a test pattern.

Using the relation of FF equivalence, FFs are partitioned into some equivalent groups. Considering the test pattern application to a combinational circuit part, the same value can be assigned to the FFs belonging to the same equivalent FF group.

The number of equivalent groups is defined as N_G.

### 3.2 Circuit modification 2

In order to make a sequential circuit be controllable in case N_PI <= N_G, we modify the circuit. The same primary input line is connected to MUXs which are connected to FFs belonging to the same equivalent group as shown in Fig.2.

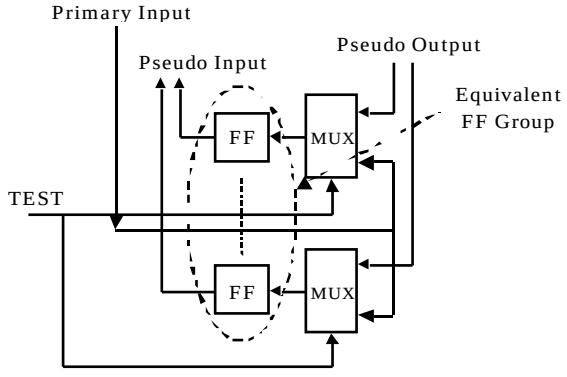


**Fig.2 Circuit modification -2**

## 4. Non-scan testable design 3

The method shown in 3 cannot be applied to the case where N_PI < N_G.

The FFs included N_PI equivalent groups are called SF1s, and the other FFs are called SF2s. In order to make a sequential circuit be controllable, we modify the circuit. SF1s are controlled using the same method as shown in Fig.2. A FF is added between one input of the MUX connected to an SF2 and a primary input. This additional FF makes it possible that an arbitrary test pattern can be set to the original FFs in two clocks.

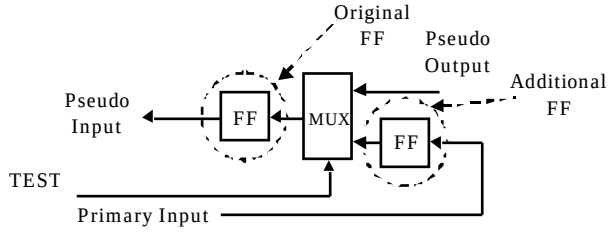


**Fig. 3 Circuit modification-3**

## 5. Experimental results

We applied the proposed method to ISCAS89 benchmark circuits. Test patterns of an original circuit and a modified circuit are generated using HITEC[3], and fault coverages are calculated. The results are shown in Tables 1, 2 and 3. We can find out that the coverages of almost all the circuits are improved.

## 6. Conclusions

We discuss a non-scan testable design for a sequential circuit by only focusing controllability. The discussed method modifies a sequential circuit so that all the FFs can be directly controlled from primary inputs in a test mode. Experimental results show that testability is improved.

We are discussing the test scheduling method for the circuit modified by the proposed method.

**Table1 Experimental results(N_PI >= N_FF)**

| Circuit Name | Original Coverage | Modified Circuit Coverage | Modified Circuit Hardware Overhead |
|---|---|---|---|
| s386 | 81.8% | 100.0% | 1.35% |
| s510 | 0.0% | 99.8% | 1.20% |
| s641 | 86.5% | 100.0% | 2.56% |
| s713 | 81.2% | 94.2% | 2.39% |
| s820 | 95.5% | 100.0% | 0.69% |
| s832 | 93.4% | 98.44% | 0.68% |
| s1488 | 93.67% | 100.0% | 0.33% |
| s1494 | 96.1% | 99.2% | 0.33% |

**Table2 Experimental results(N_PI >= N_G)**

| Circuit Name | Original Coverage | Modified Circuit Coverage | Modified Circuit Hardware Overhead | No of FF Groups |
|---|---|---|---|---|
| s953 | 8.25% | 100.0% | 2.83% | 16 |
| s1196 | 99.8% | 99.7% | 1.41% | 14 |
| s1238 | 94.7% | 95.2% | 1.36% | 14 |
| s5378 | 68.35% | 95.1% | 3.28% | 35 |

**Table3 Experimental results(N_PI < N_G)**

| Circuit Name | Original Coverage | Modified Circuit Coverage | Modified Circuit Hardware Overhead | No of FF Groups |
|---|---|---|---|---|
| s298 | 86.04% | 99.76% | 19.83% | 8 |
| s344 | 93.57% | 99.78% | 5.30% | 10 |
| s349 | 94.00% | 99.35% | 5.24% | 10 |
| s382 | 73.93% | 98.58% | 30.65% | 12 |
| s444 | 66.88% | 91.35% | 15.56% | 8 |
| s526 | 9.19% | 96.32% | 33.62% | 13 |
| s1423 | 38.15% | 84.44% | 6.66% | 25 |
| s9234 | 0.46% | 75.29% | 8.45% | 38 |
| s13207 | 6.17% | 78.00% | 4.05% | 35 |

**References**

[1] V. Chickermane, E.M.Rudnick, P. Banerjee and J. H. Patel,"Non-scan design-for-testability techniques for sequential circuits," *Proc. of 30th ACM/IEEE Design Automation Conference*, pp.236-241, 1993.

[2] S. Ohtake, T. Masuzawa and H. Fujiwara."A Non-Scan DFT Method for Controllers to Achieve Complete Fault Efficiency," *Proc. of h 7th Asian Test Symposium*, pp. 204-211, 1998.

[3] .T. Niermann and J. H. Patel,"HITEC: A Test Generation Package for Sequential Circuits," *Proc. of European Design Automation Conference*, pp. 214-218, 1991.