ETW'01 Tutorials

Tutorial 1: Test Challenges in Nanometer Technologies

Presenter 1:	Presenter 2:
SANDIP KUNDU	**RAJESH GALIVANCHE**
Intel Corporation	Intel Corporation
Sandip.Kundu@ieee.org	Rajesh.Galivanche@intel.com

DATE: **Tuesday, May 29**
TIME: **9:00 – 17:00**

AUDIENCE: IC designers, test engineers, and their managers, also researchers, test methodology developers and test tool developers.

SUMMARY: Testing has to address manufacturing defects, process marginalities and design marginalities. The techniques for addressing defects is still evolving while techniques for addressing process marginalities and design marginalities are at their infancy. This tutorial will give an overview of the state of the art in all three areas. The tutorial begins with an introduction to device and interconnect scaling and their implications and then moves on to strategies for dealing with emerging issues such as defect based testing and testing for process and design marginality related failures.

KEYWORDS: Manufacturing Defects, Interconnect Shorts-Opens, Process Variation, Interconnect Coupling Impedance, Soft Error Technology Scaling, Defect Density

Tutorial 2: Built-In Self-Test for Chips and System-on-a-Chip

Presenter And Co-Author:
JANUSZ RAJSKI
Mentor Graphics Corporation
rajski@mentor.com

Co-Author:
JERZY TYSZER
Poznan University of Technology

DATE: **Tuesday, May 29**
TIME: **9:00 – 17:00**

AUDIENCE: Designers of complex systems-on-a-chip, IP core providers and integrators, test engineers, researchers, and managers interested in learning about state-of-the-art BIST technology, practices and automation tools.

SUMMARY: This tutorial presents state-of-the-art BIST technology, practices and automation tools. It discusses compelling reasons as well as common barriers for its adoption. It covers guidelines for design of BIST-able cores, techniques for random pattern testability, as well as BIST architectures for random logic and memory arrays. Special emphasis is placed on issues related to at-speed testing, and BIST schemes for multi-frequency designs with on-chip generated clocks. The tutorial presents hierarchical BIST methodology for systems on silicon, based on BIST-ready IP cores and system BIST integration. Finally, the tutorial presents automation of BIST synthesis illustrated with applications and case studies. Attendees receive hard copies and a CD-ROM of the presented material.

KEYWORDS: Logic Built-In Self Test, Scan, BIST-Ability Rules and Guidelines, Random Pattern Testability, Generators of Pseudorandom Patterns, Compactors of Responses, BIST Schemes, At-Speed Multi-Frequency Testing, Memory BIST, BIST Automation

ETW'01 Technical Program

TUESDAY, May 29, 2001

8:00 - 9:00 : TUTORIALS AND WORKSHOP REGISTRATIONS

9:00 - 17:30 : TUTORIALS

Tutorial 1: Test Challenges in Nanometer Technologies
Presenters: S. Kundu and R. Galivanche - Intel, USA

Tutorial 2: Built-In Self-Test for Chips and System-on-a-Chip
Presenter: J. Rajski - Mentor Graphics, USA

16:00 - 18:30 : WORKSHOP REGISTRATION

18:30 - 20:00 : WELCOME RECEPTION

FRINGE TECHNICAL MEETINGS

Tuesday, May 29, 10:00 – 16:00

SEDA (Swedish EDA Committee) meeting
Zebo Peng - zpe@ida.liu.se

Tuesday, May 29, 20:00 – 22:30

ETTTC meeting
Christian Landrault - landraul@lirmm.fr

Friday, June 1, 16:00 – 21:00

ETW'01 proceedings paper selection m'eeting
Hans-Joachim Wunderlich
wu@informatik.uni-stuttgart.de

ETW'01 Technical Program

WEDNESDAY, May 30, 2001

7:30 - 8:30 : WORKSHOP REGISTRATION

8:30 - 10:00 : OPENING

Welcome
Z. Peng, General Chair
Linköping University, S

Program Introduction
H.-J. Wunderlich, Program Chair
University of Stuttgart, D

Keynote Address
A Test- and Debug-Friendly Reuse Architecture
R. Payne – Philips Semiconductors, San Jose, USA

Abstract

This presentation describes the concepts behind a skeleton of reuse which addresses a wide range of System-on-a-Chip problems, including test and design debug. The talk addresses the ways that the on-chip communication architecture is being driven to create a timing closure friendly, testable, and debugable design. These approaches are being reflected in the "Nexperia" platforms and provide "Architecting Flexibility".

10:00 - 11:00 : POSTER SESSION P1 & COFFEE BREAK

Testing of Analog and Digital Circuits

Moderators:
F. Azais – LIRMM/University of Montpellier, F
E. Gramatova – Slovak Technical University, SK

P1.1 A Design Technique for High-Performance Self-Checking Combinational Circuits
E. Dubrova – Royal Institute of Technology, S

P1.2 On-Line BIST Experiments for Distributed Systems
L. Miclea, Sz. Enyedi, R. Orghidan – Technical University of Cluj-Napoca, RO

P1.3 Impact of Spot Defects on Fault Modeling and Tests in Dual-Port Memories
S. Hamdioui, A.J. van de Goor, D. Eastwick, M. Rodgers – Delft University of Technology, NL

P1.4 ADC Testing By Means of Stochastic Signal
J. Holub, J. Vedral – Czech Technical University, CZ

P1.5 Speed-up Techniques for Fault-based Analogue Fault Simulation
Y. Kilic, M. Zwolinski – University of Southhampton, UK

11:00 - 12:30 : SESSIONS 1A and 1B

Session 1A

Defect-Oriented Testing

Moderators:
H. Manhaeve – Qstar, B
S. M. Reddy – University of Iowa, USA

1A.1 Analysing Bridging Faults Impact on EEPROM Cell Array
J. M. Portal, A. Perez – ICF/L2MP, F

1A.2 Internal Feedback Bridging Faults in Combinational CMOS Circuits: Analysis and Testing
Y. Miura, S. Seno – Tokyo Metropolitan University, JP

1A.3 Failure Analysis on Logic Devices using ATPG Tool
C. Burmer, P. Egger – Infineon Technologies, D

Session 1B – Industrial Practice:

System-Level DFT

Moderators:
M. Lobetti-Bodoni – Siemens ICN SpA, I
T. Koivunkangas – Nokia, SF

1B.1 Applying RTL Design-for-Test Rules Checking to Reduce Cycle Time
H. Lang, N. Scott – Motorola, D

1B.2 Using Zoo - A System Simulation Framework to Build a Boundary Scan Verification Platform
S. Andersson – Ericsson, S

1B.3 System-Level DfT for Consumer Products
D.C.L. van Geest, F. G. M. de Jong – Philips, NL

12:30 - 14:00 : LUNCH

14:00 - 15:30 : SESSIONS 2A and 2B

Session 2A:

Delay Testing

Moderators:
B. Becker – University of Freiburg, D
K. Kinoshita – Osaka Gakuin University, JP

2A.1 A Fault Model for Function and Delay Testing
J. Yi, J.P. Hayes – University of Michigan, USA

2A.2 Reducing the Susceptibility of Design-for-Delay-Testability Structures to Process- and Application-Induced Variations
H.J. Vermaak, H.G. Kerkhoff – University of Twente, NL

2A.3 Demodulation Based Testing of Off Chip Driver Performance
W. Daehn – Hochschule Magdeburg, D

Session 2B – Industrial Practice:

Core-based Testing and P1500

Moderators:
D. Gizopoulos – University of Piraeus, GR
E. J. Marinissen – Philips Research, NL

2B.1 IEEE P1500: what should we do about it?
Y. Zorian – LogicVision, USA;
R. Kapur – Synopsys, USA;
E. J. Marinissen – Philips, NL

2B.2 The New Challenge in Core-Based Testing
G. Francis – Philips Semiconductors Southampton, UK

2B.3 Designing Hierarchical Test Access Controllers for Embedded Cores using IEEE P1500 and VSIA Compliant Architectures
B.I. Dervisoglu – Cadence Design Systems, USA

15:30 - 16:30 : POSTER SESSION P2 & COFFEE BREAK

Scan Based Test & Testability

Moderators:
A. Benso – Politechnico di Torino, I
B. Al-Hashimi – University of Southampton, UK

P2.1 A Low Cost Test Scheme Using Random Test Sessions for Scan-Based BIST
T. Maeda, S. M. Reddy – University of Iowa, USA;
K. Kinoshita – Osaka Gakuin University, JP

P2.2 DRAFT: A Scanning Test Methodology for Dynamic and Partially Reconfigurable FPGAs
M.G. Gericota, G.R. Alves – ISEP, P;
M.L. Silva, J.M. Ferreira – FEUP, P

P2.3 Interactive Tool for Behavioral Level Testability Analysis
Z. Kotasek, R. Ruzicka, J. Strnadel – Technical University of Brno, CZ;
J. Hlavicka – Czech Technical University, CZ

16:30 - 18:00 : SESSIONS 3A and 3B

Session 3A – Industrial Practice:

Case Studies

Moderators:
B. Bennetts – Bennetts Assoc., UK
P. Muhmentaler – Infineon Technologies, D

3A.1 A Microcontroller with Embedded DRAM and Test Features
P. Goddard, R. McConnell – Infineon Technologies, D

3A.2 Design-for-Test Strategy for the Nexperia™ Digital Video Platform System Chips (short paper)
S. Oostdijk, F. Bouwman – Philips Semiconductors, USA;
B. Vermeulen – Philips Research, NL

3A.3 Design-for-Debug Strategy for the Nexperia™ Digital Video Platform System Chips (short paper)
B. Vermeulen – Philips Research, NL;
S. Oostdijk, F. Bouwman – Philips Semiconductors, USA

3A.4 Automated Regression Testing of CTI-Systems
O. Niese, T. Margaria, A. Hagerer – METAFrame Technologies, D;
B. Steffen – University of Dortmund, D;
G. Brune, W. Goerigk, H.-D. Die – Siemens, D

Session 3B – Industrial Practice:

Full Scan

Moderators:
W.-T. Cheng – Mentor Graphics, USA
A. Singh – Auburn University, USA

3B.1 Moving from One Pass Scan Synthesis to One Pass DFT Synthesis
M. Hirech, S. Ramnath – Synopsys, USA

3B.2 OPMISR: Accelerated Scan with On-Product Signatures
C. Barnhart, B. Keller, B. Koenemann,
R. Walther – IBM Microelectronics, USA

3B.3 Enhanced Reduced Pin-Count Test for Full-Scan Design
H. Vranken, T. Waayers –
Philips Research, NL;
H. Vincent, D. Lelouvier –
Philips Semiconductors, F

18:30 - 20:30 : DINNER

20:30 - 22:00 : SESSION 4

Evening Breakout Session

Moderator:
C. Landrault – LIRMM, F

The participants will join one of the "breakout groups" to brainstorm, in a friendly atmosphere, on one of the following topics:

- Low-Cost DFT-Enabled Testers – Why Haven't We Used Them Before?
- Testing of Microsystems: Challenge or Common Knowledge?
- Mixed Signal Testing: What are the Objectives?
- Useful Academic Research in Test: A Contradiction in Terms?

THURSDAY, MAY 31, 2001

8:30 - 10:00 : SESSIONS 5A and 5B

Session 5A

Analog and Mixed-Signal Testing

Moderators:
M. Renovell – LIRMM, F
B. Straube – Fraunhofer Institute, D

5A.1 Reducing Analogue Fault-Simulation Time by Using High-Level Modelling in Dotss for an Industrial Design
L. Fang, H.G. Kerkhoff – University of Twente, NL;
G. Gronthoud – Philips Research, NL

5A.2 On-Chip Signal Level Evaluation for Mixed-Signal ICs using Digital Windows Comparators
D. De Venuto – Politecnico di Bari, I;
M. J. Ohletz – Alcatel Microelectronics, B;
B. Ricco – University of Bologna, I

5A.3 Steady-State D.C. Domain Equivalent Faults - A Potentiometric DAC Case Study
M. Worsman, M.W.T. Wong, Y.S. Lee – Hong Kong Polytechnic University, PRC

Session 5B – Industrial Practice:

Transportation of Test Data

Moderators:
P. Prinetto – Politechnico di Torino, I
J. P. Teixeira – INESC, P

5B.1 Test Wrapper and Test Access Mechanism Co-Optimization for System-on-a-Chip
V. Iyengar, K. Chakrabarty – Duke University, USA

5B.2 A Packet Switching Communication-Based Test Access Mechanism for System Chips
M. Nahvi, A. Ivanov –
University of British Columbia, CAN

5B.3 Project Results from Implementation of Direct Link between ATPG and ATE for Structural Test Using IEEE 1450
P. Burlison, J. Doege, R. Dokken –
Inovys Corporation, USA;
I. Burgess – Mentor Graphics, USA

10:00 - 11:00 : POSTER SESSION P3 & COFFEE BREAK

Test generation and Testability Analysis

Moderators:
W. Anheier – University of Bremen, D
S. Chiusano – Politecnico di Torino, I

P3.1 Binary Decision Diagrams and Testability Measures
K. Wiklund –
Ericsson Radio Systems AB, S

P3.2 Fast Static Compaction of Test Sequences Using Implications and Greedy Search
J. Raik, A. Jutman, R. Ubar –
Tallinn Technical University, EE

P3.3 Test Pattern Generation Using a New VHDL Open Platform on Behavioural Level
J. Stefanovic, P. Miklos,
E. Gramatova, M. Fischerova –
Slovak Technical University, SK

P3.4 On Combinational Redundancy and Identification of Undetectable Faults in Synchronous Sequential Circuits
M. Enamul Amyeen, I. Pomeranz,
W. K. Fuchs – Purdue University, USA

11:00 - 12:00 : SESSIONS 6A and 6B

Session 6A

System-Level Testing

Moderators:
I. Phillips – ARM,UK
I. Teixeira – INESC, P

6A.1 From UML to EOP Functional Test: Just a Dream or a Feasible Industrial Approach?
Baldini, A. Benso, P. Prinetto –
Politecnico di Torino, I;
S. Mo, A. Taddei – Magneti Marelli
Electronic Division, I

6A.2 System Level Diagnosis - A Comparison of Two Alternative Approaches
M. Khalil, C. Robach – LCIS, F;
F. Novak, A. Zuzek – Josef Stefan Institute
Ljubljana, SL

Session 6B – Industrial Practice:

Hierarchical DFT

Moderators:
X. Gu – Cisco Systems, USA
G. Francis – Philips Semiconductors, UK

6B.1 Using a Hierarchical DfT Methodology in High Frequency Processor Designs for Improved Delay Fault Testability
M. Kessler, G. Kiefer, J. Leenstra,
K. Schünemann, T. Schwarz – IBM, D;
H.-J. Wunderlich – University of Stuttgart, D

6B.2 An Evolution to a DFT-Centric Test Paradigm that Scales with Technology Progress
W. Radermacher, J. Rivoir –
Agilent Technologies, USA

12:00 - 12:45 : SESSION 7

Report on Breakout Session
C. Landrault, LIRMM, F

13:00 - 14:30 : LUNCH on BOAT
(Beginning of the social event)

14:30 - 23:30 : SOCIAL EVENT & DINNER

FRIDAY, JUNE 1, 2001

8:30 - 10:00 : SESSIONS 8A and 8B

Session 8A

RTL Validation, DFT and TPG

Moderators:
M. Kessler – IBM, D
R. Ubar – Tallin Technical University, EE

8A.1 RTL Design Validation, DFT and Test Pattern Generation
M. B. Santos, F.M. Gonçalves, I.C. Teixeira, J. P. Teixeira – IST/INESC, P

8A.2 On RTL Scan Design
Y. Huang, C.-C. Tsai, N. Mukherjee, W.-T. Cheng, S. M. Reddy – University of Iowa, USA

8A.3 An Implementation for Test-Time Reduction in VLIW TTA Architectures
V. A. Zivkovic , H. G. Kerkhoff – University of Twente, NL

Session 8B – Industrial Practice:

Memory Testing

Moderators:
J. Vollrath – Infineon Technologies, USA
Y. Zorian – LogicVision, USA

8B.1 Improving the Programming Time of Flash Memories on Assemblies for High-Volume Production
A. Biewenga – Philips Research, NL

8B.2 A Tool for Highly Dependable SRAMs Generation
F. Bigongiari – Aurelia Microelectronica, I;
S. Chiusano, G. Di Natale, P. Prinetto – Politecnico di Torino, I

8B.3 The IEEE P1581 SCITT Working Group, Scope and Status
F. de Jong, L. van de Logt – Philips Research, NL

10:00 - 11:00 : POSTER SESSION P4 & COFFEE BREAK

BIST and Power consideration

Moderators:
P. Girard – LIRMM, F
H. Vranken – Philips, NL

P4.1 Advanced Evolution of Nonlinear Cellular Automata for Combinational BIST
J. Bingham, J. Muzio – University of Victoria, CAN

P4.2 System-on-Chip Test Parallelization Under Power Constraints
E. Larsson, Z. Peng – Linköping University, S

P4.3 Controlling BIST for System-On-Chip
M.-L. Flottes, J. Pouget, B. Rouzeyre – LIRMM/University of Montpellier, F

P4.4 CA-CSTP: A Flexible Architecture for Low-Power BIST of Sequential Circuits
F. Corno, M. Rebaudengo, M. Sonza Reorda, M. Violante – Politecnico di Torino, I

11:00 - 12:30 : SESSIONS 9A and 9B

Session 9A

BIST and Test Resource Partitioning

Moderators:
J. Rajski – Mentor Graphics, USA
M. Fischer – Agilent, D

9A.1 Two-Dimensional Test Data Compression for Scan-Based Deterministic BIST
H.-G. Liang, H.-J. Wunderlich –
University of Stuttgart, D;
S. Hellebrand – University of Innsbruck, A

9A.2 On Hardware Generation of Random Single Input Change Test Sequences
R. David – INP Grenoble;
P. Girard, C. Landrault, S. Pravossoudovitch,
A. Virazel – LIRMM, F

9A.3 Reusing Scan Chains for Test Pattern Decompression
R. Dorsch, H.-J. Wunderlich –
University of Stuttgart, D

Session 9B – Industrial Practice:

Mixed-Signal Testing

Moderators:
G. Krampl – Infineon Technologies AG, A
A. Richardson – Lancaster University, UK

9B.1 A VHDL-based Virtual Test Concept for Pre-silicon Test-program Debug
Marco Rona, Gunter Krampl –
Infineon Technologies AG, A

9B.2 Using At-Speed BIST to Test LVDS ser/des Function
M. Eckersand, F. Franzon, K. Filliter –
National Semiconductor, S

9B.3 Extending Core Test Methodology to the Analog/Mixed-Signal Domain
C. Feige – Philips Semiconductors, NL
G. Seuren – Philips Research, NL

12:30 - 14:00 : LUNCH

14:00 - 15:30 : SESSIONS 10

Industrial Practice:

Logic BIST in Action

Moderators:
G. Carlsson – Ericsson, S
S. Hellebrand – University of Innsbruck, A

10.1 A Fast Timing Closure Technique for Industrial Use of Logic BIST
X. Gu, S. S. Chung, F. Tsang –
Cisco Systems, USA
J.A. Tofte, H. Rahmanian –
Mentor Graphics, USA

10.2 Logic BIST Technology Evaluation. An Industrial Case Study
C. Feige – Philips Semiconductors, NL;
J. Geuzebroek –
Delft University of Technology, NL

10.3 Can Commercial Tools Handle DFT of Digital SoCs?
K. Petersen – HDC AB, S;
O. Andersson – Ericsson Radio Systems, S

15:30 - 15:40 : CLOSING SESSION